

Quanta Project Name: XM2

Dell Project Name: Reebok

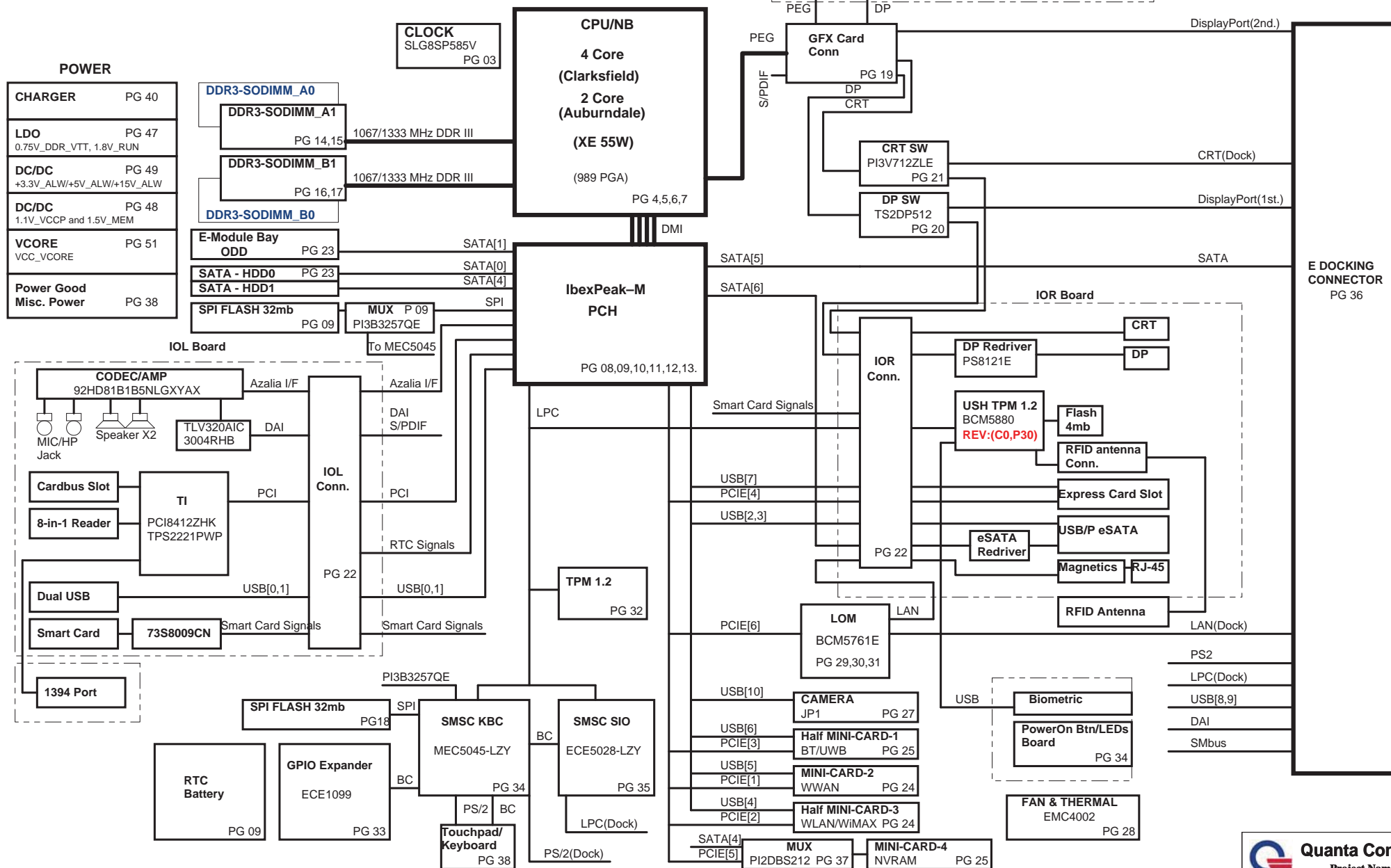
X00(SS1) Stage

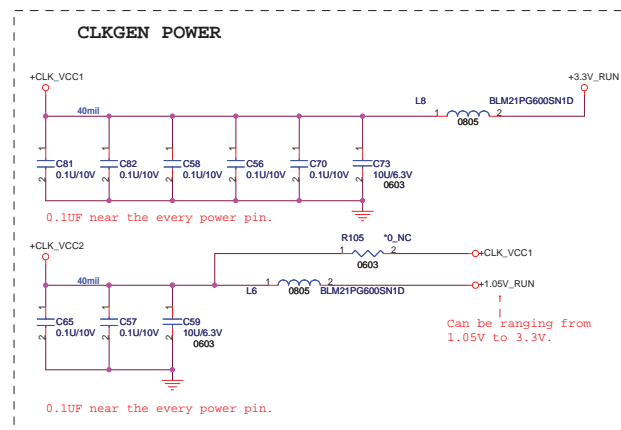
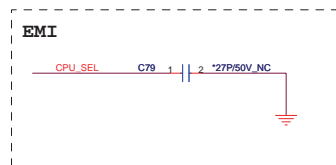
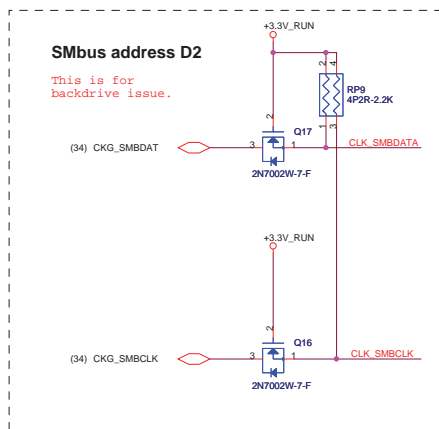
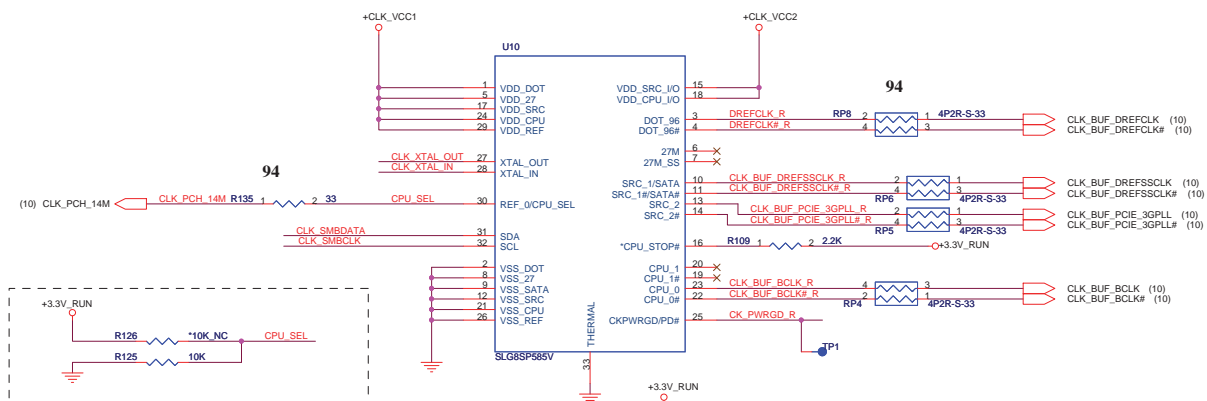
BOARD REV : A

2009-03-03

System Block Diagram of Reebok

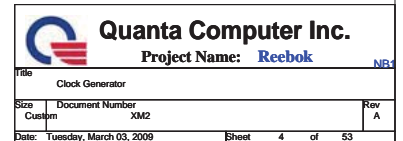
PWA XXX, PWB XXX,
SCHEM XXX.
Board Ver : A
Date:20081201





AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

For EMI request, will NC at A00.

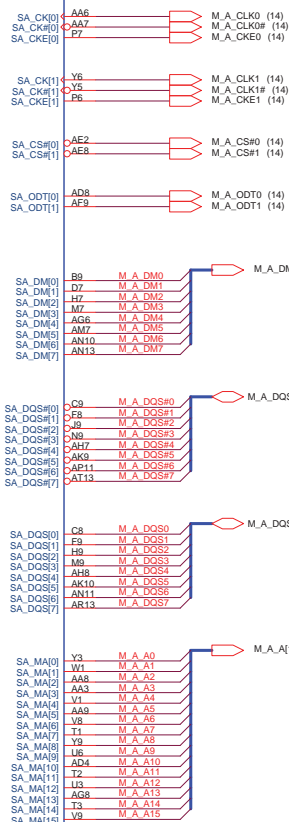


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

U17C

SA_DQ[0] A10
SA_DQ[1] C10
SA_DQ[2] A7
SA_DQ[3] A7
SA_DQ[4] B10
SA_DQ[5] D10
SA_DQ[6] E10
SA_DQ[7] A8
SA_DQ[8] DA
SA_DQ[9] E10
SA_DQ[10] E6
SA_DQ[11] E7
SA_DQ[12] E9
SA_DQ[13] B7
SA_DQ[14] E7
SA_DQ[15] C6
SA_DQ[16] H10
SA_DQ[17] DA
SA_DQ[18] K7
SA_DQ[19] J8
SA_DQ[20] G7
SA_DQ[21] G10
SA_DQ[22] J7
SA_DQ[23] J0
SA_DQ[24] L7
SA_DQ[25] M6
SA_DQ[26] M6
SA_DQ[27] L6
SA_DQ[28] L6
SA_DQ[29] K6
SA_DQ[30] N8
SA_DQ[31] P8
SA_DQ[32] A8
SA_DQ[33] A8
SA_DQ[34] A8
SA_DQ[35] A8
SA_DQ[36] A8
SA_DQ[37] A8
SA_DQ[38] A8
SA_DQ[39] A8
SA_DQ[40] A8
SA_DQ[41] A8
SA_DQ[42] A8
SA_DQ[43] A8
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SA_DQ[47] A8
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SA_DQ[58] A8
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SA_DQ[63] A8

DDR SYSTEM MEMORY A

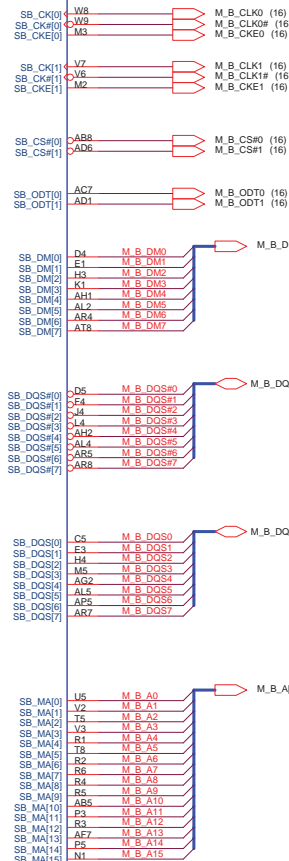


P298927-3641-01F

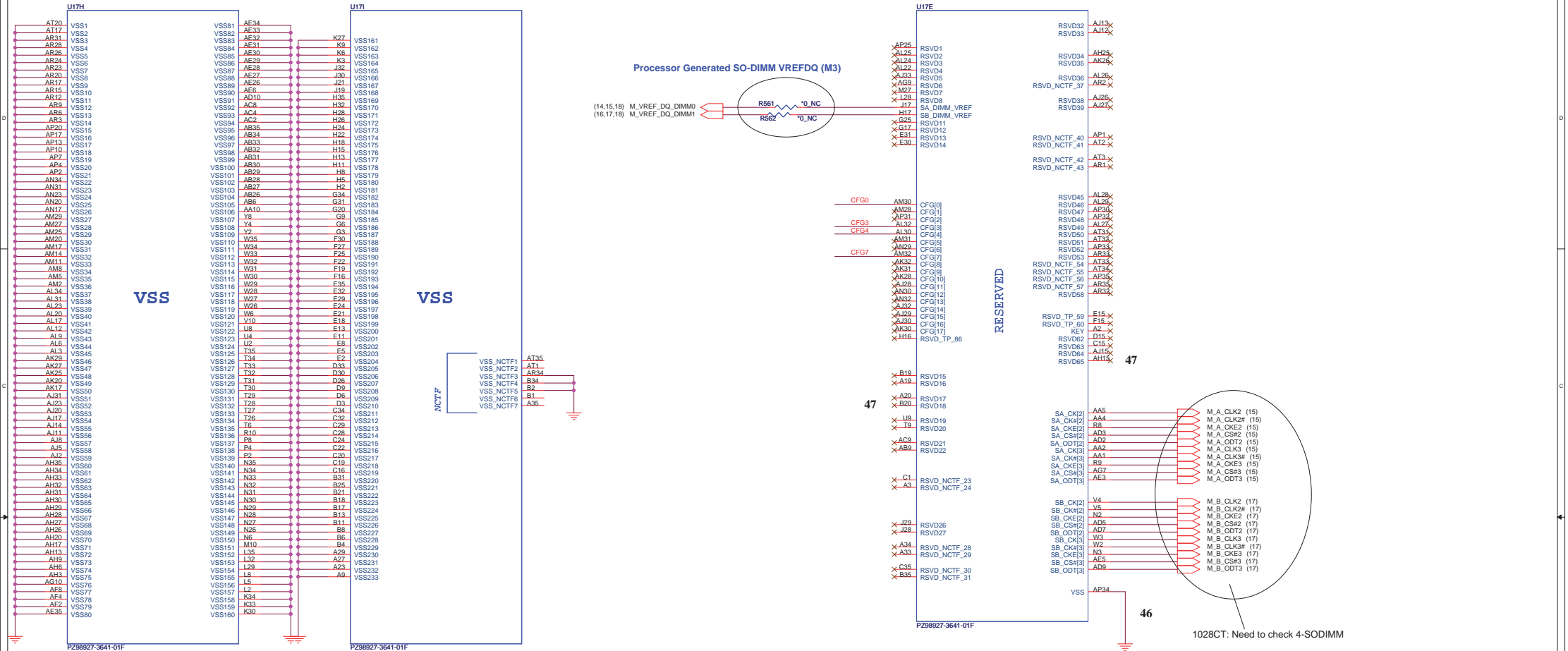
U17D

SB_DQ[0] B5
SB_DQ[1] A5
SB_DQ[2] C3
SB_DQ[3] B3
SB_DQ[4] E4
SB_DQ[5] A6
SB_DQ[6] A4
SB_DQ[7] C4
SB_DQ[8] D1
SB_DQ[9] D2
SB_DQ[10] E1
SB_DQ[11] F1
SB_DQ[12] C2
SB_DQ[13] F5
SB_DQ[14] F3
SB_DQ[15] G4
SB_DQ[16] H6
SB_DQ[17] G2
SB_DQ[18] J6
SB_DQ[19] J3
SB_DQ[20] G1
SB_DQ[21] G5
SB_DQ[22] J1
SB_DQ[23] J5
SB_DQ[24] L3
SB_DQ[25] L3
SB_DQ[26] M1
SB_DQ[27] M1
SB_DQ[28] K4
SB_DQ[29] K4
SB_DQ[30] M4
SB_DQ[31] N6
SB_DQ[32] A3
SB_DQ[33] A3
SB_DQ[34] A3
SB_DQ[35] A3
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SB_DQ[63] A3

DDR SYSTEM MEMORY B

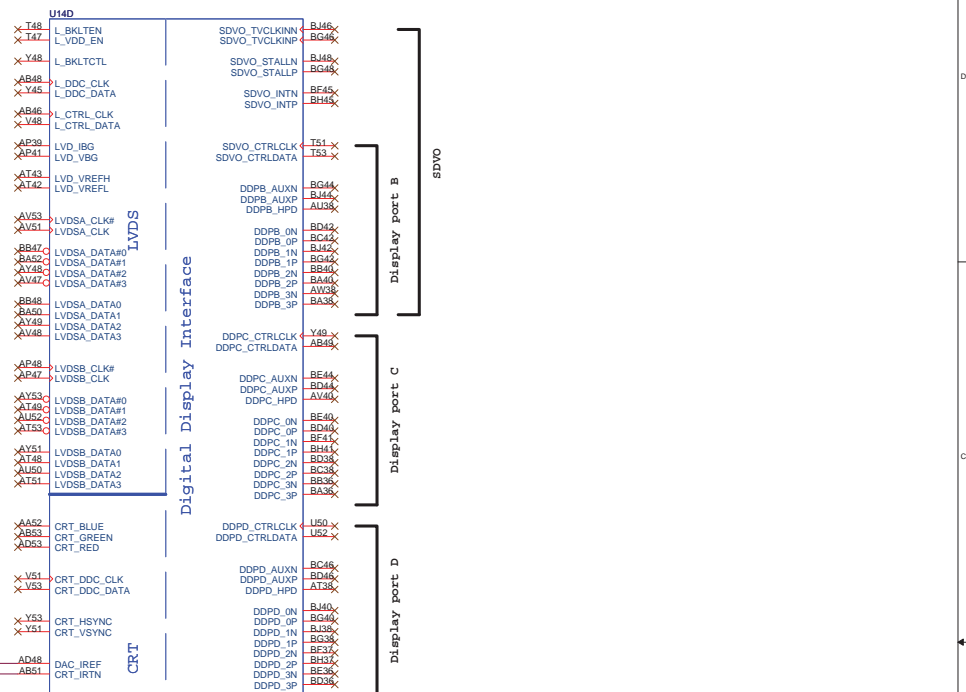
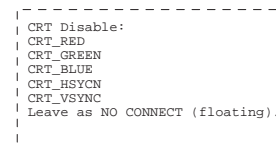


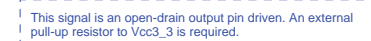
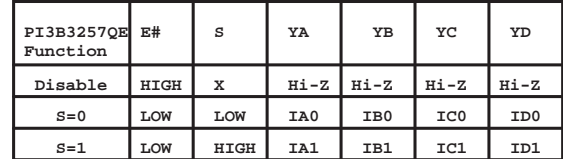
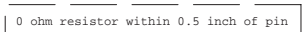
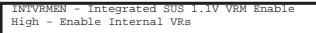
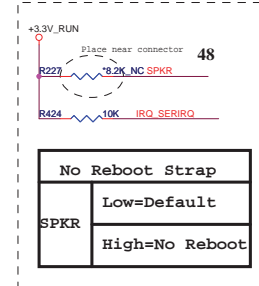
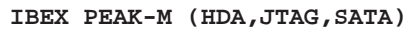
P298927-3641-01F



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed
CFG7 Clarkfield (only for early samples pre-ES1)	Common motherboard design	For early samples pre-ES1 CFD

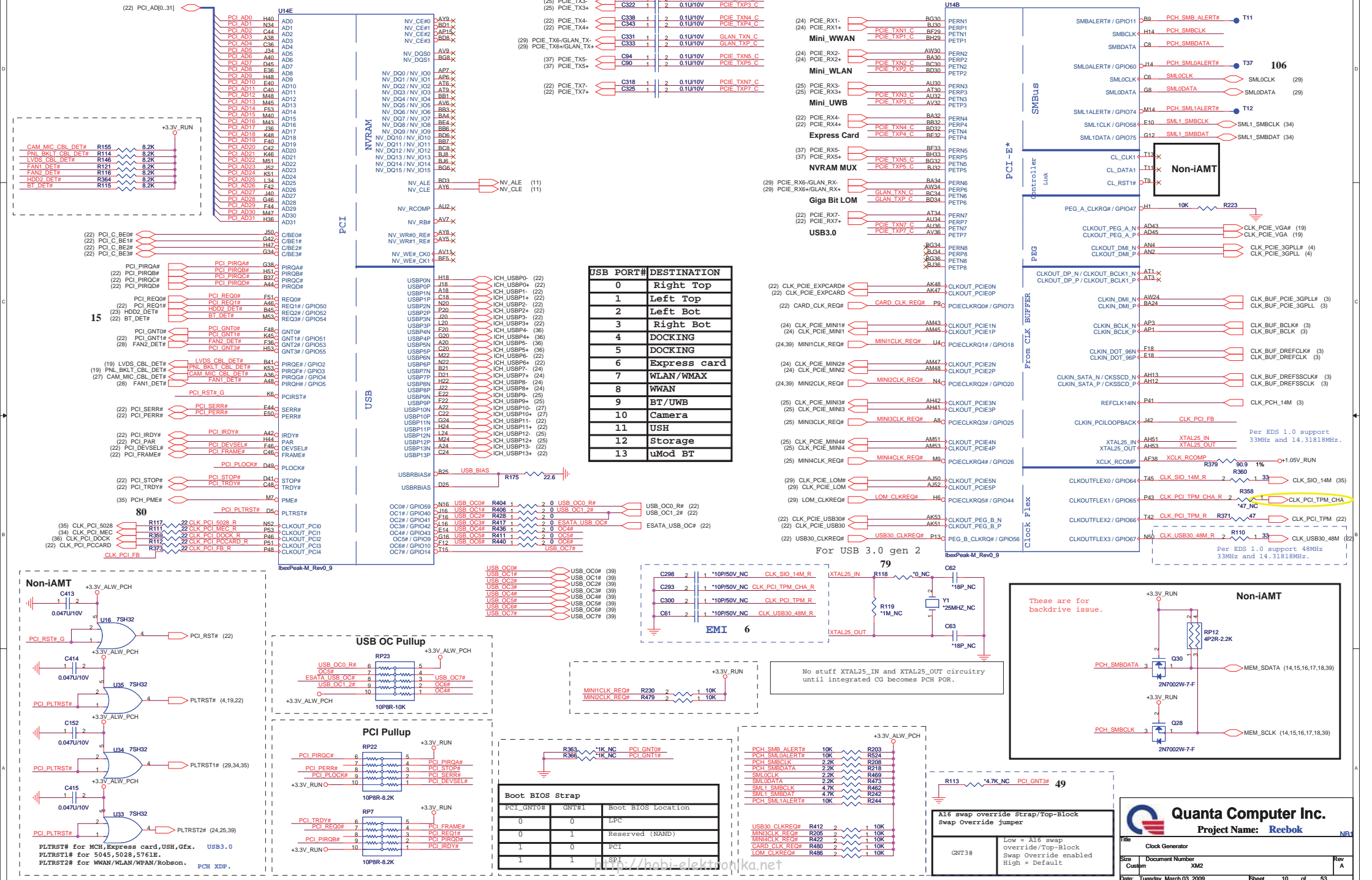
IBEX PEAK-M (LVDS,DDI)



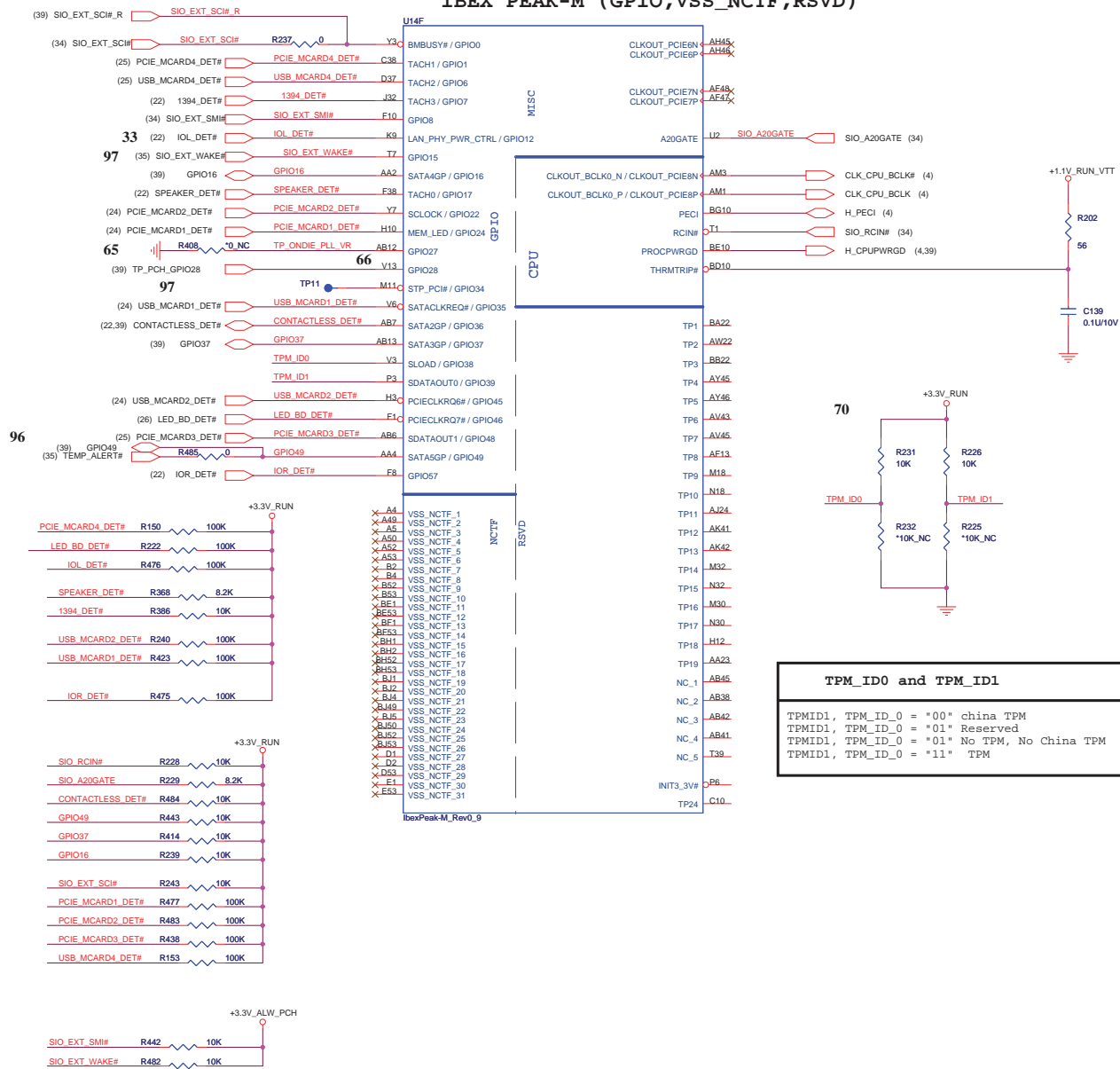


IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



50

+V_NVRAM_VCCO

(10) NV_ALE

(10) NV_CLE

R233

R236

8.2K NC

8.2K NC

DMI Termination Voltage

NV_CLE

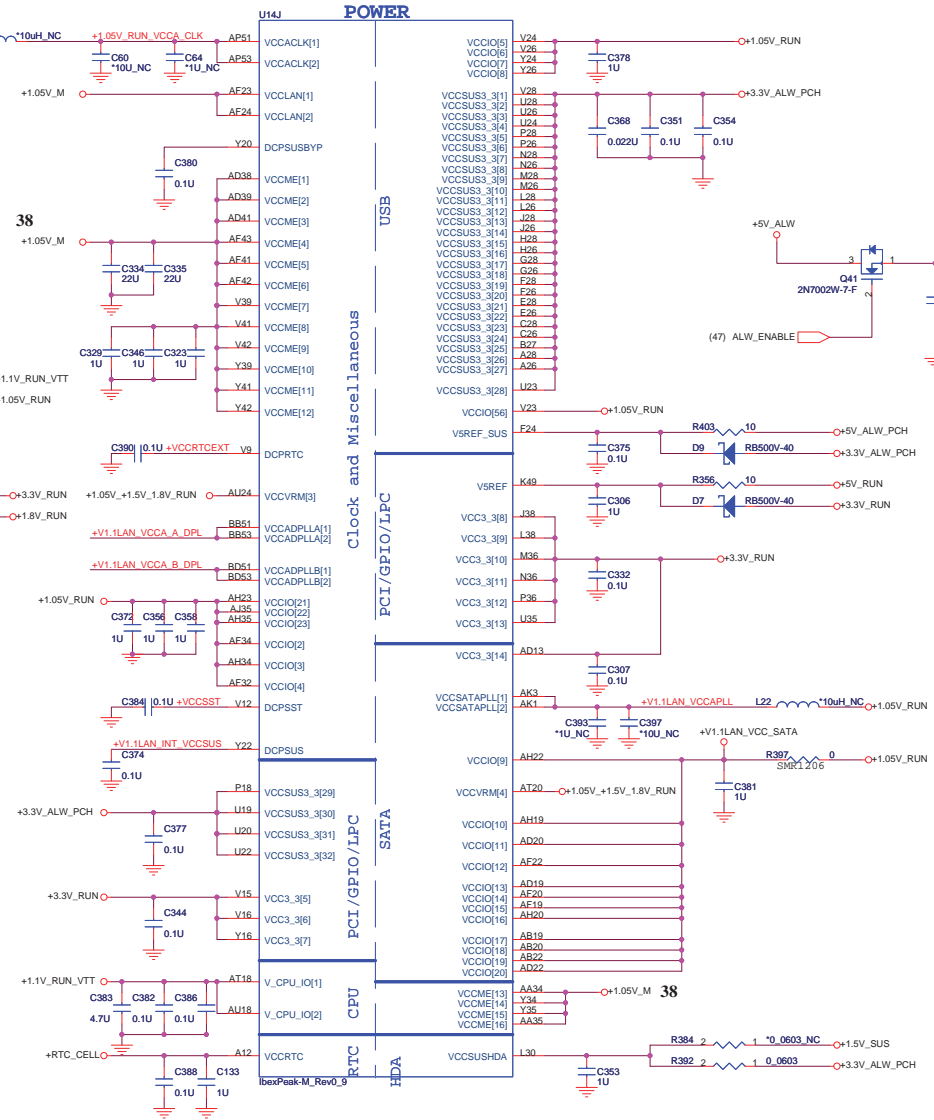
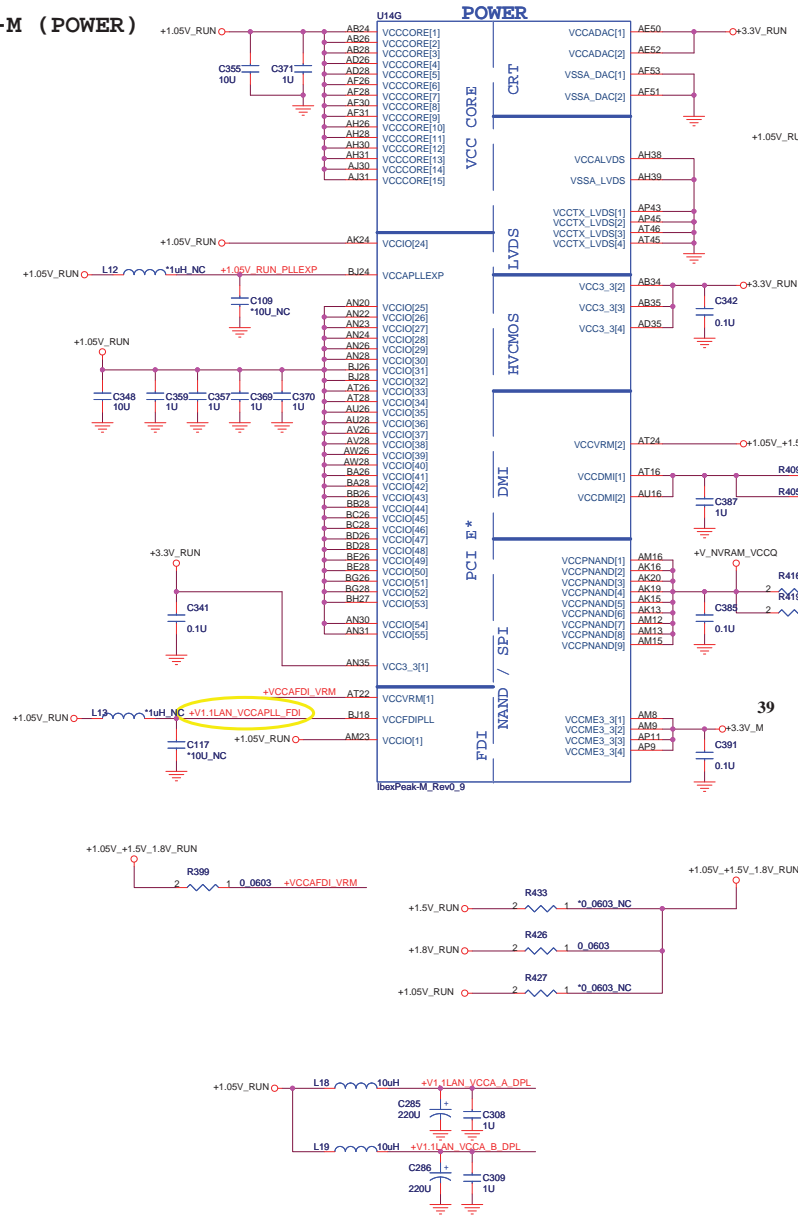
Set to Vcc when LOW
Set to Vcc/2 when HIGH

Danbury Technology Enabled

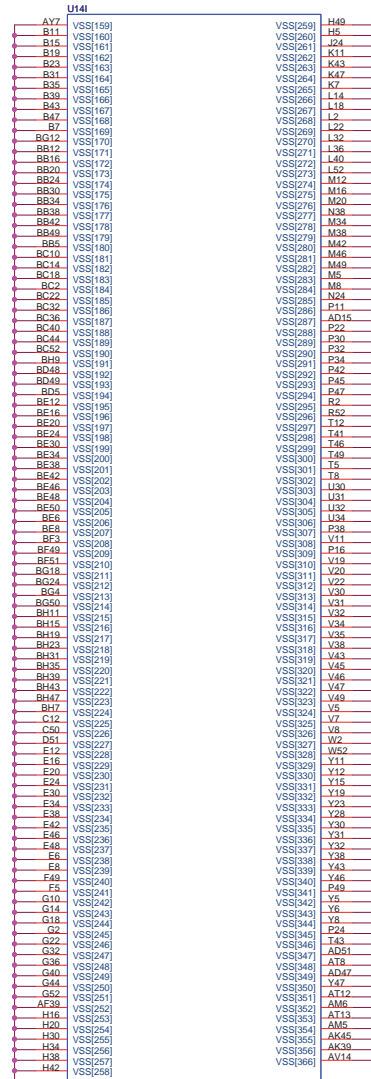
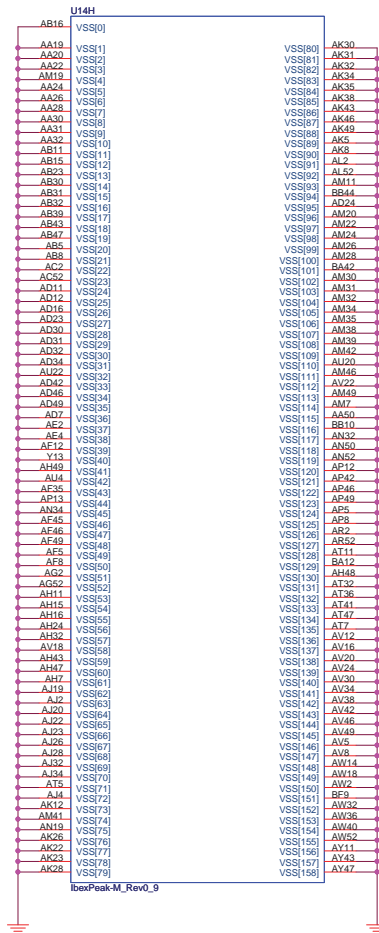
NV_ALE

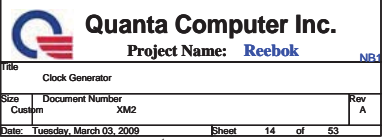
High = Enable(Default)
Low = Disable

IBEX PEAK-M (POWER)

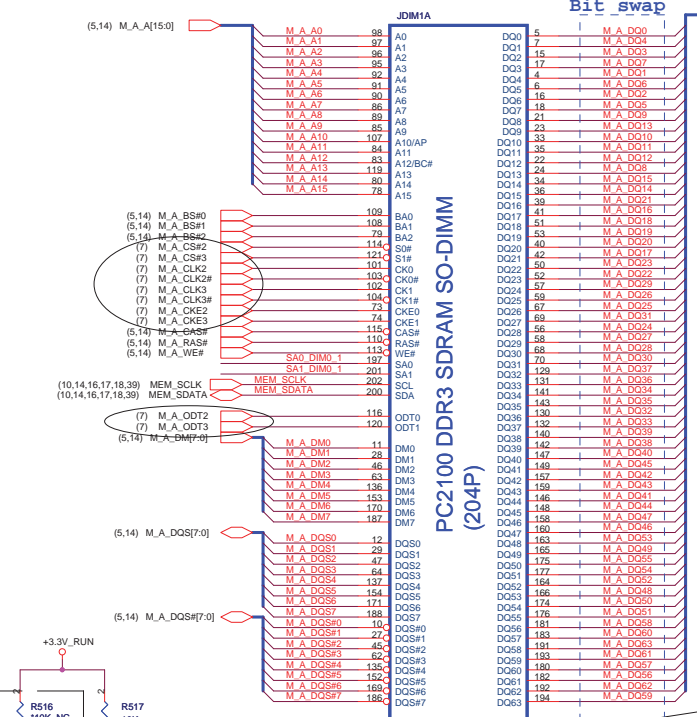


IBEX PEAK-M (GND)





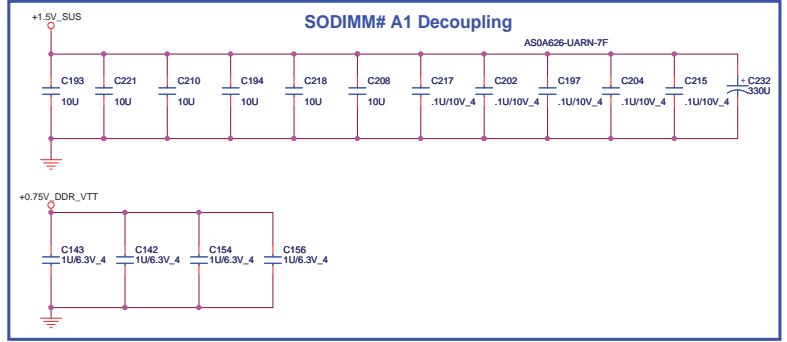
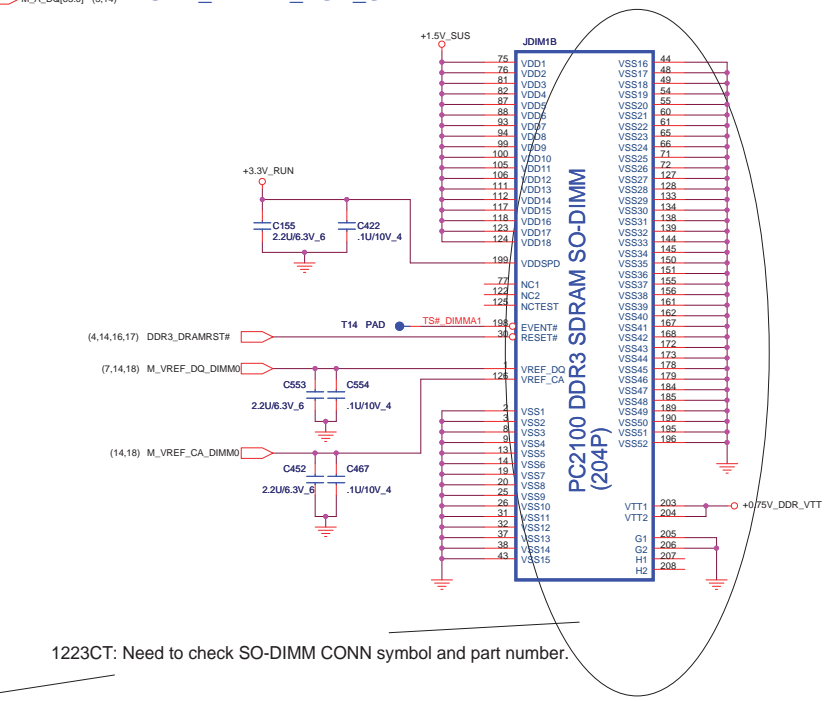
0105CT: Update JDIM1 footprint to 9.2mm, RVS type.



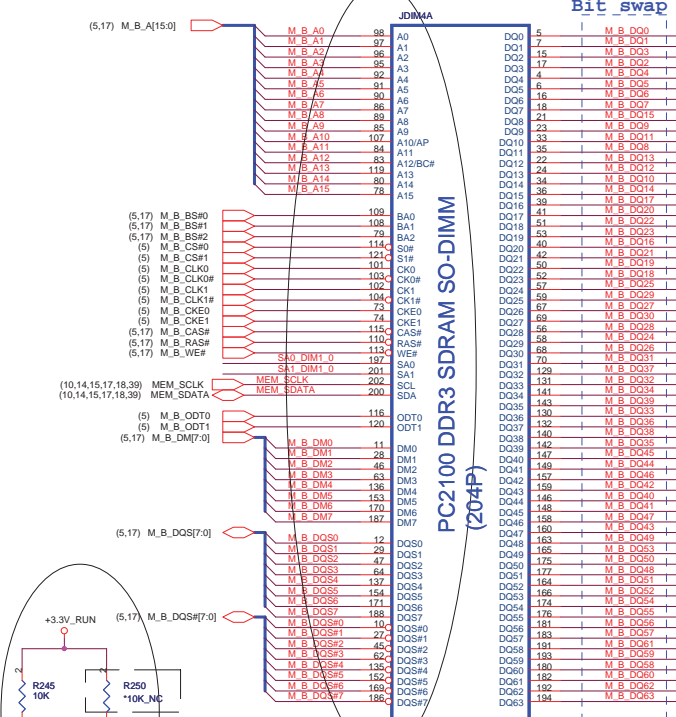
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

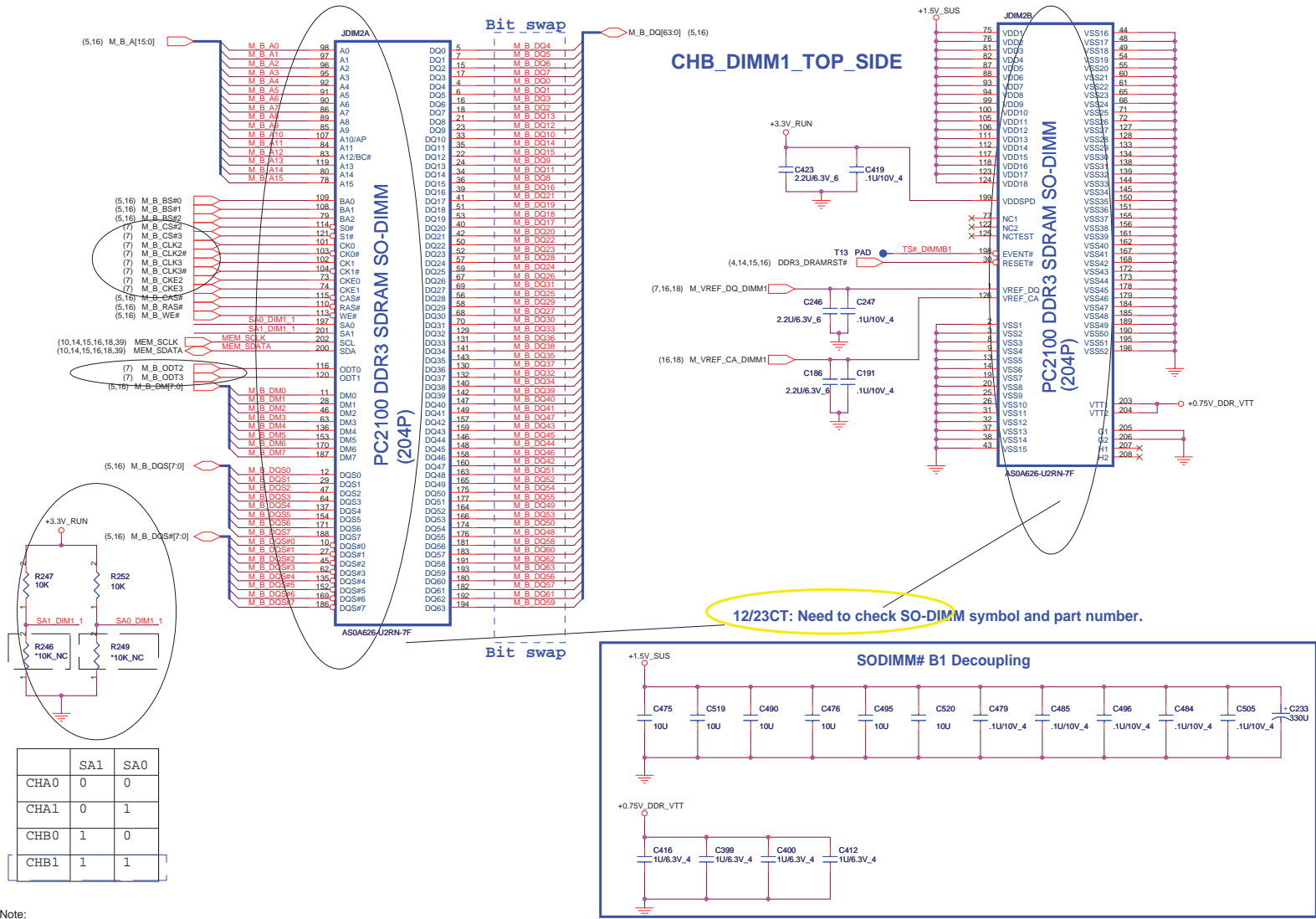
Note:
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

CHA_DIMM1_TOP_SIDE

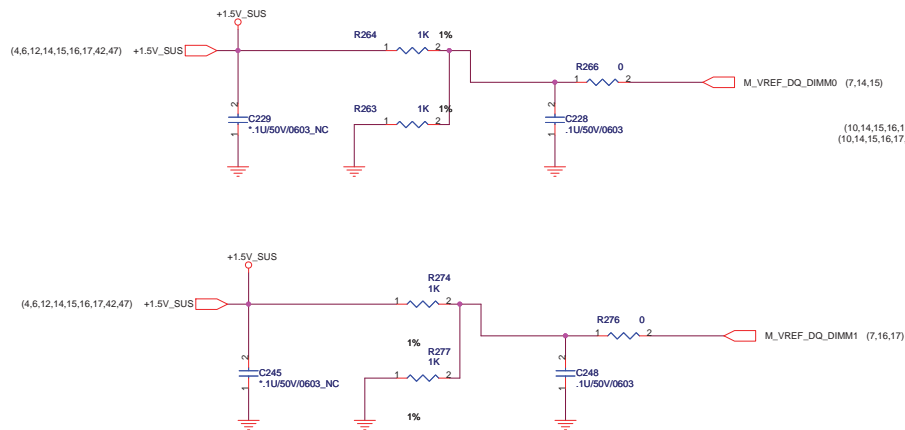


0105CT: Update JDIM4 footprint 5.2mm, STD type.



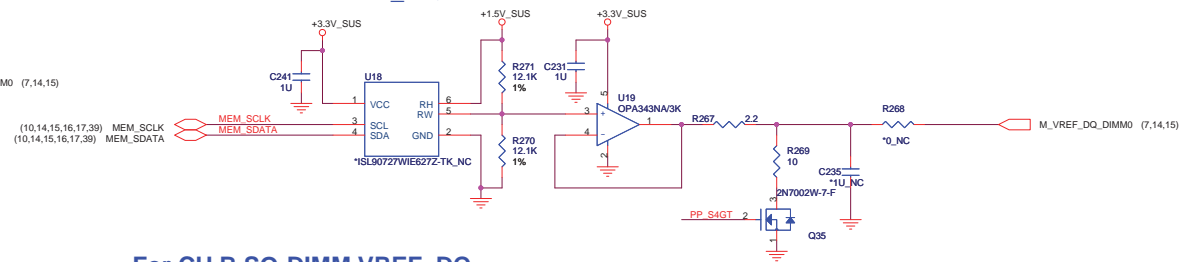


Fixed SO-DIMM VREF_DQ (M1): Default

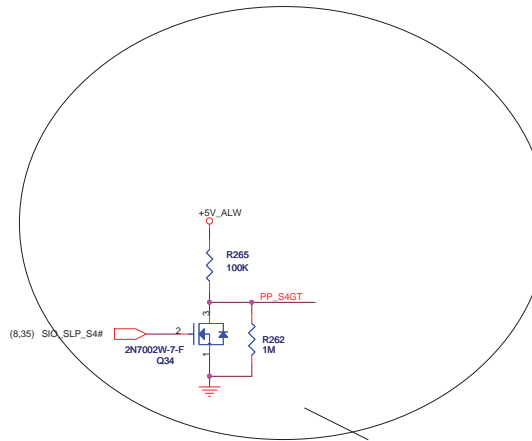
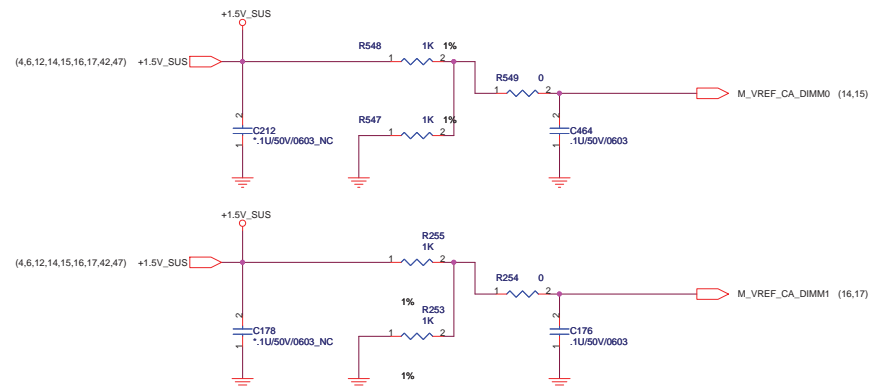
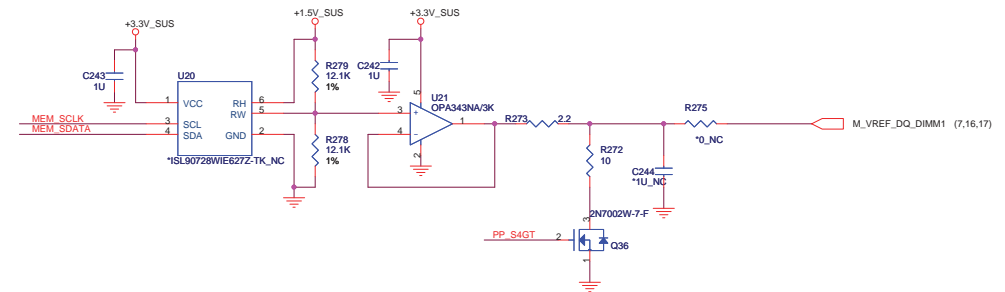


Programmable SO-DIMM VREFDQ (M2).

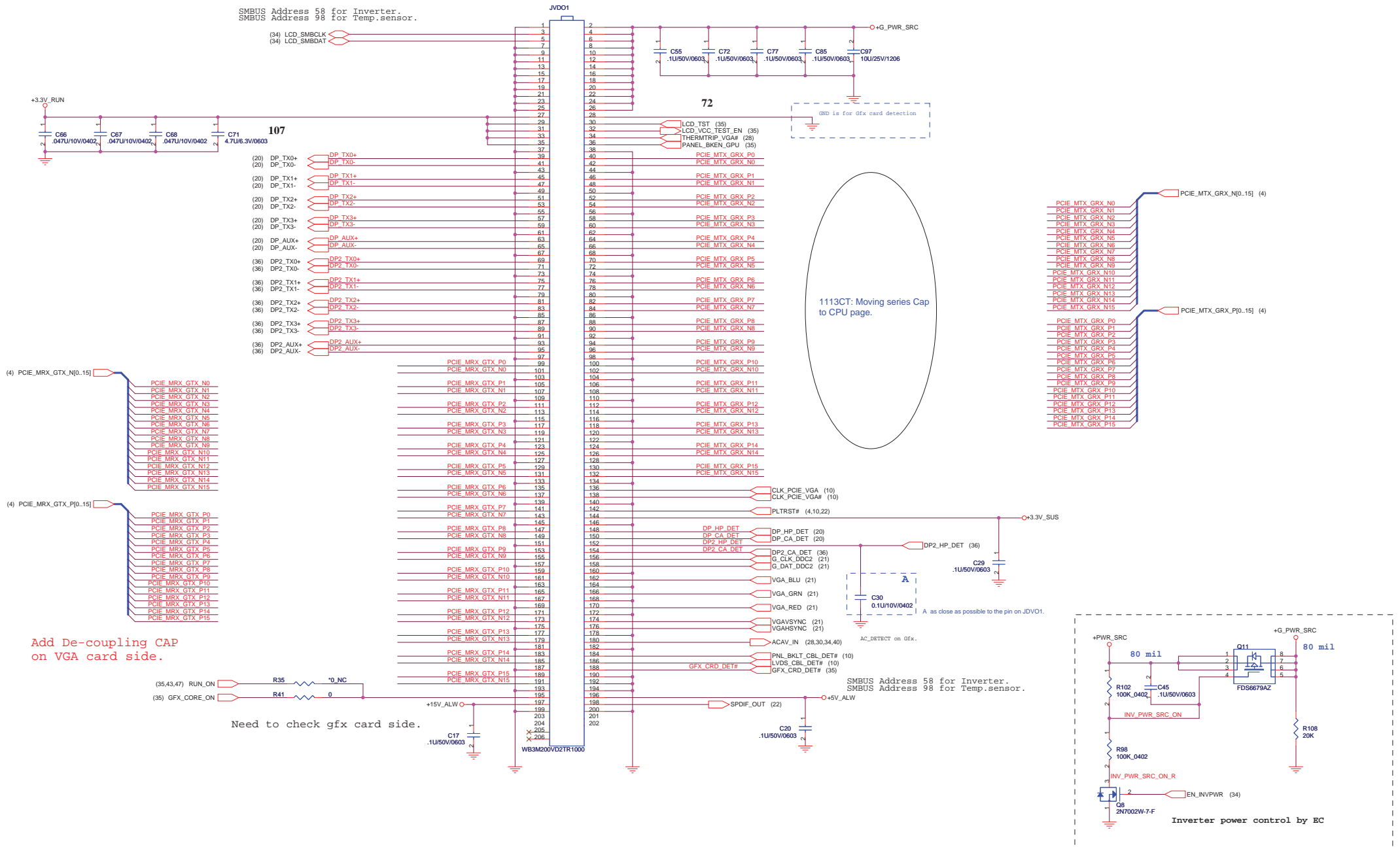
For CH A SO-DIMM VREF_DQ

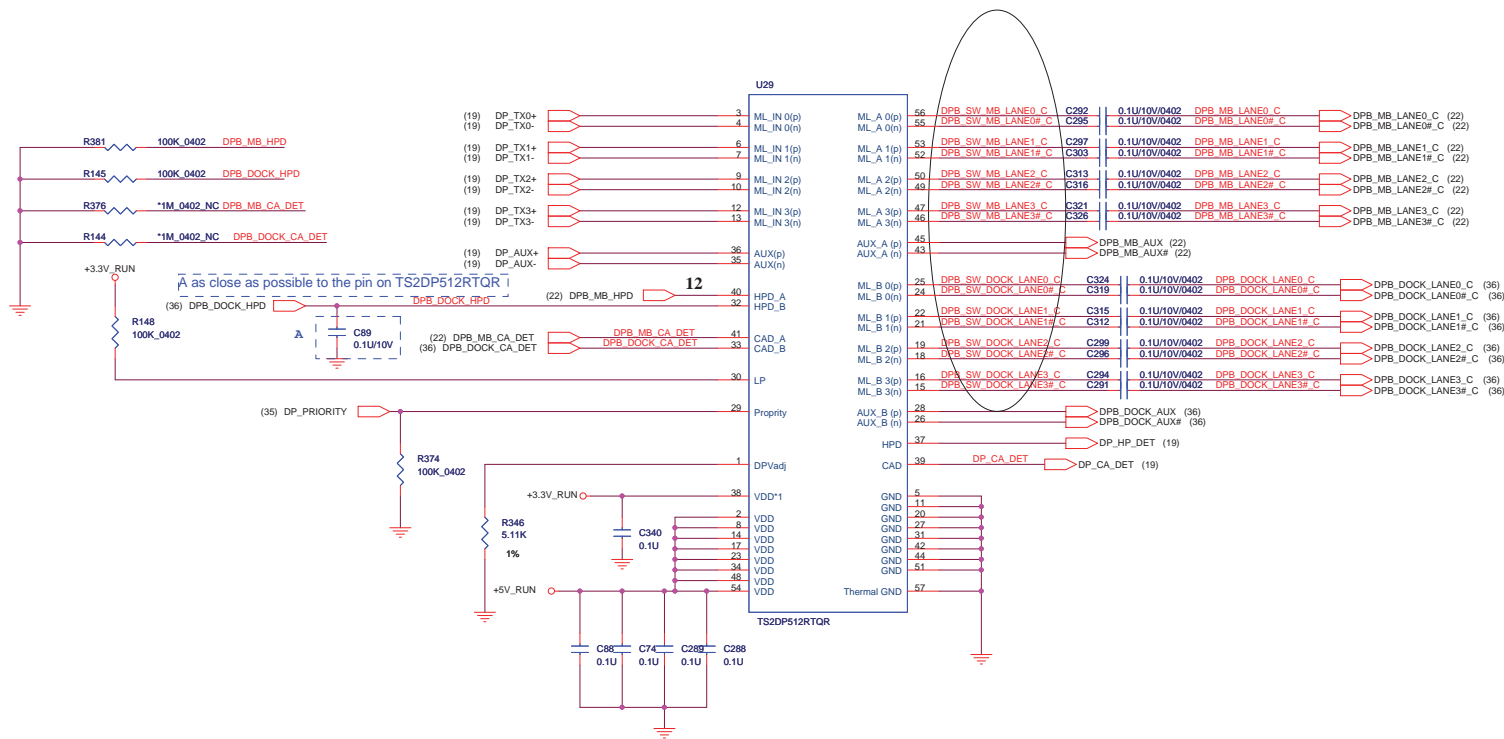


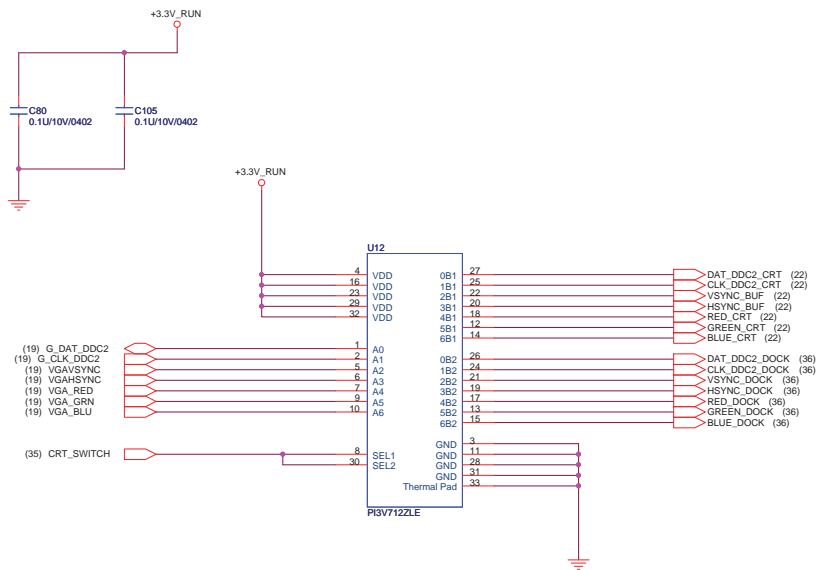
For CH B SO-DIMM VREF_DQ



1203CT: Refer to FM6C

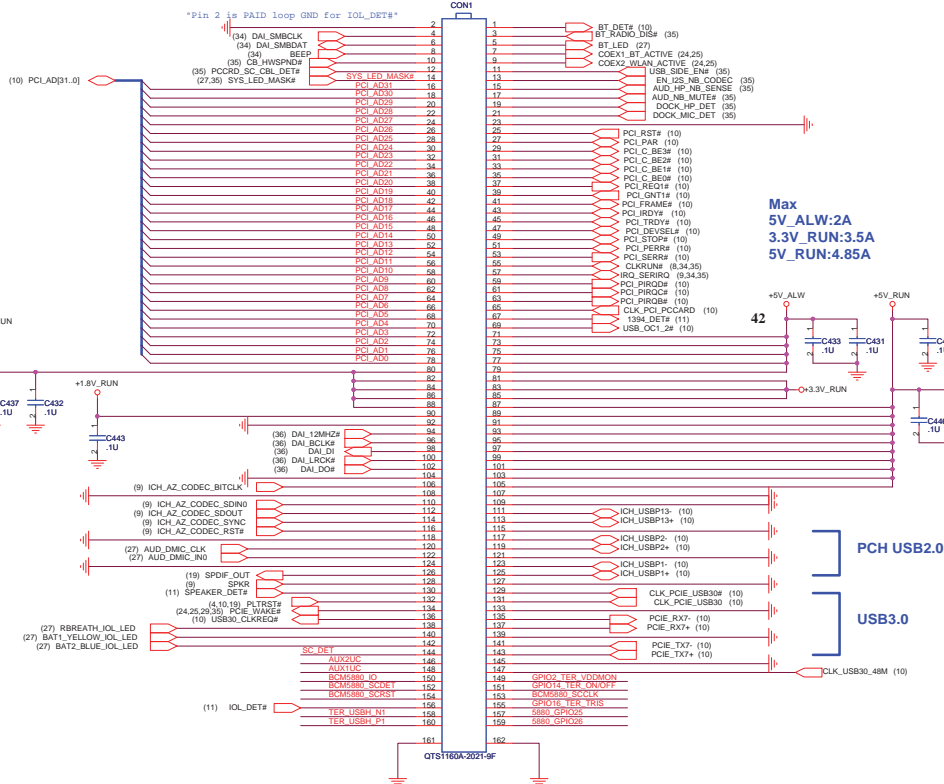






Input SELx	Input/Output An	Function	
L	nB1	An=nB1	nB2 hing impedance mode
H	nB2	An=nB2	nB1 hing impedance mode

IOL CONNECTER



Max
5V_ALW:2A
3.3V_RUN:3.5A
5V_RUN:4.85A

eSATA + USB

New added.

US\$ 5880

PCH USB2.0

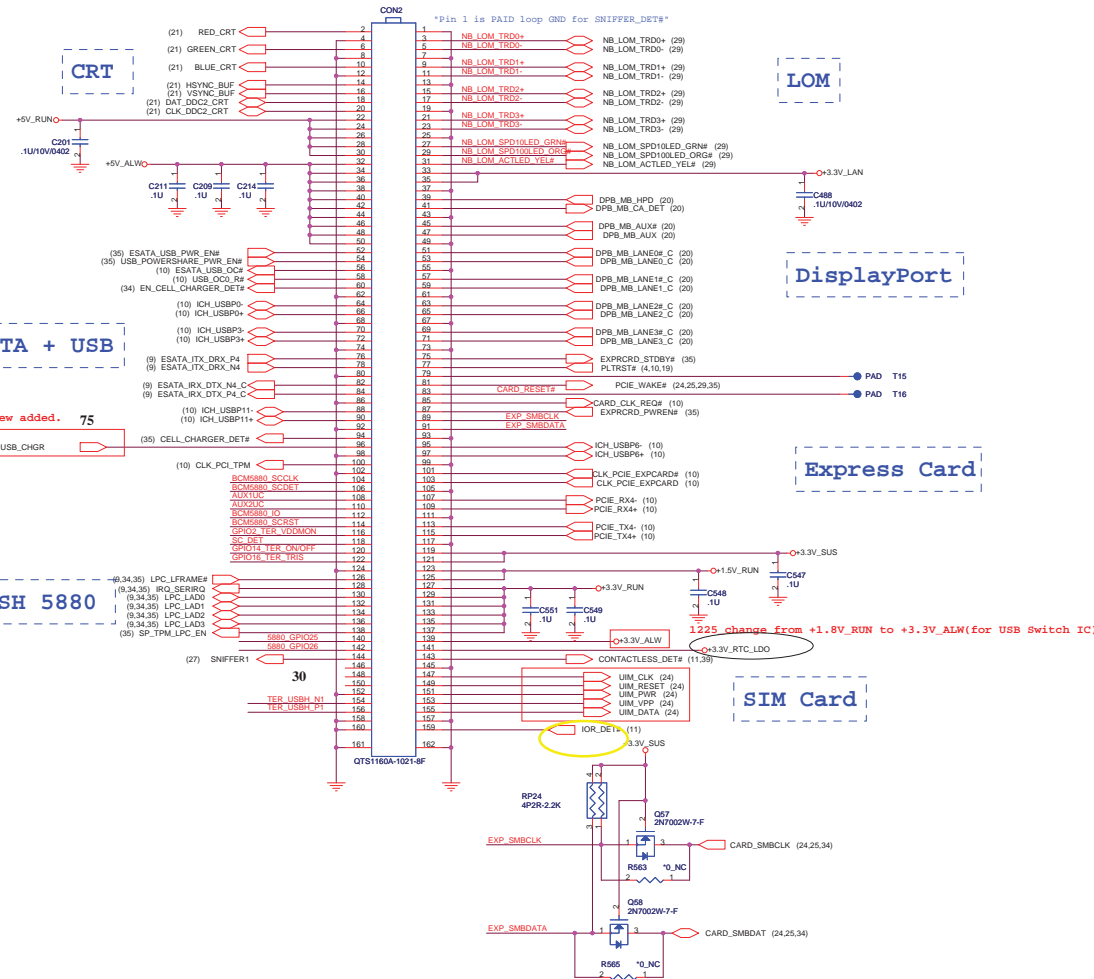
—

USB3.0

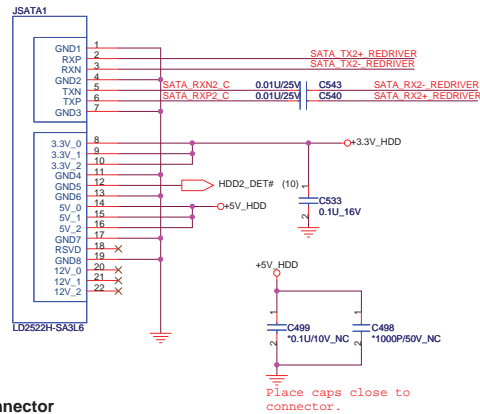
CLK_USB30_48M (10)

| As close as possible to CON1.

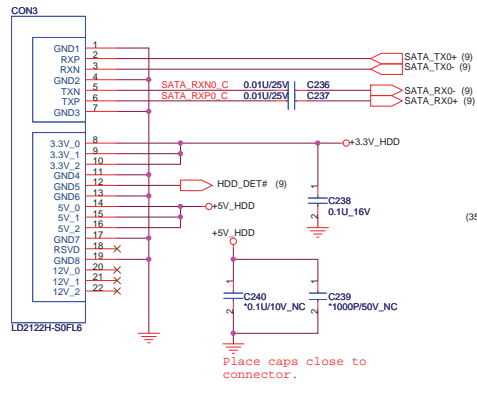
IOR CONNECTER



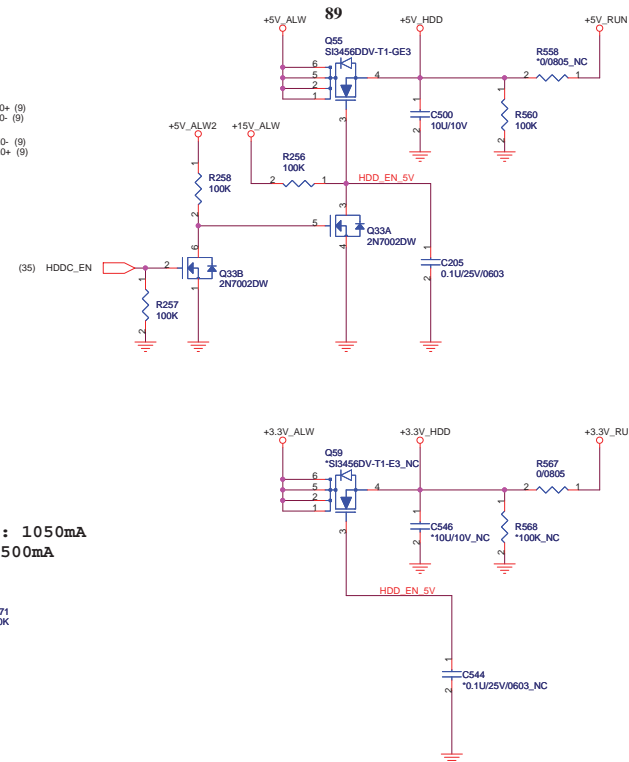
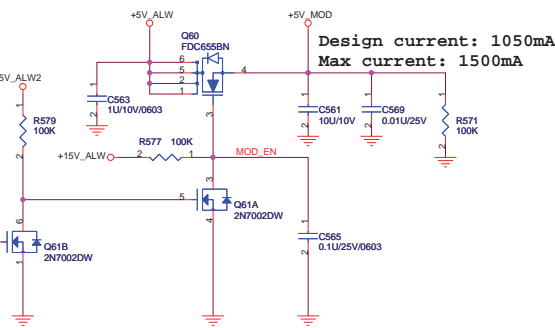
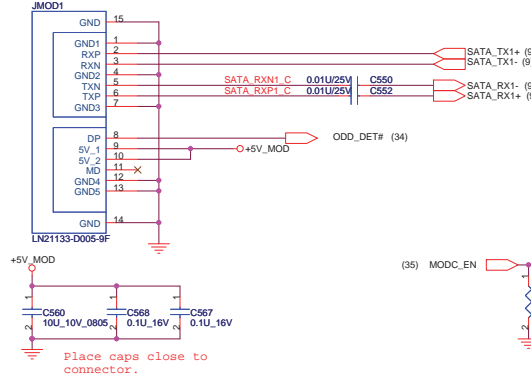
SATA (HDD1) Connector - side



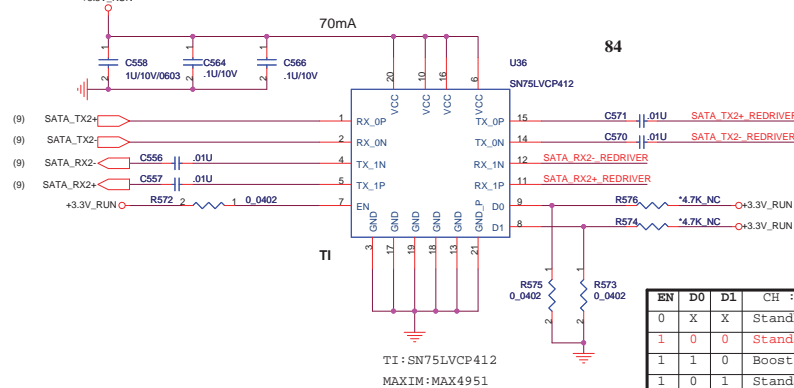
SATA (HDD0) Connector - front



ODD Connector



ESATA Re-driver.(TI-SN75LVCP412RTJR)



84

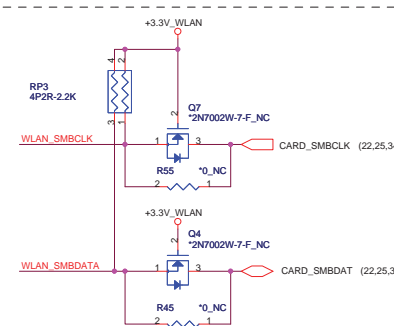
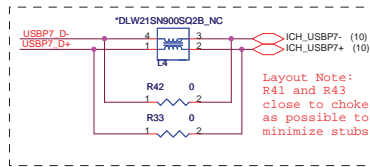
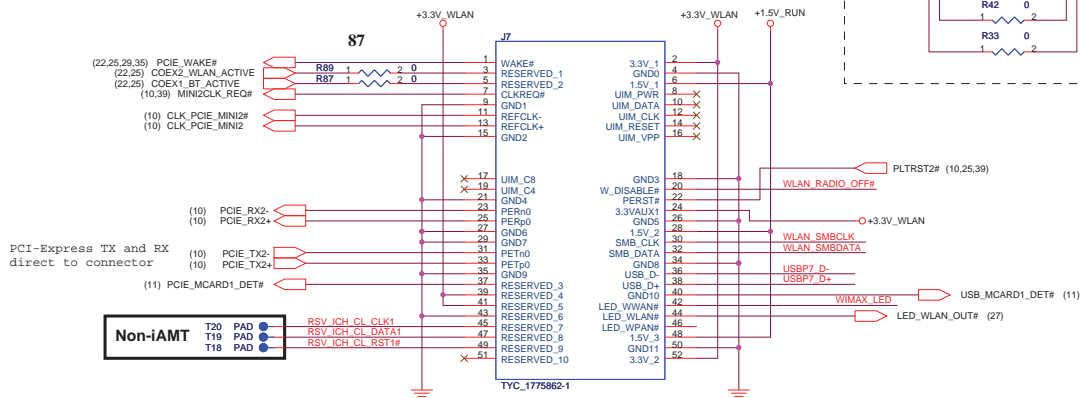
EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

Symbol:

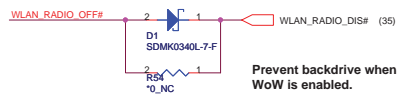
2N7002W-7-F



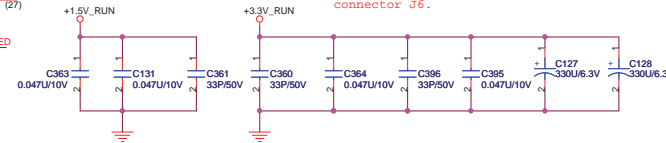
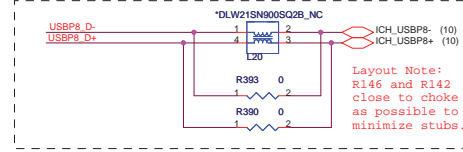
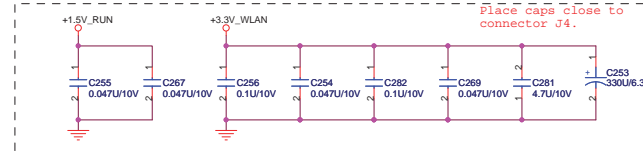
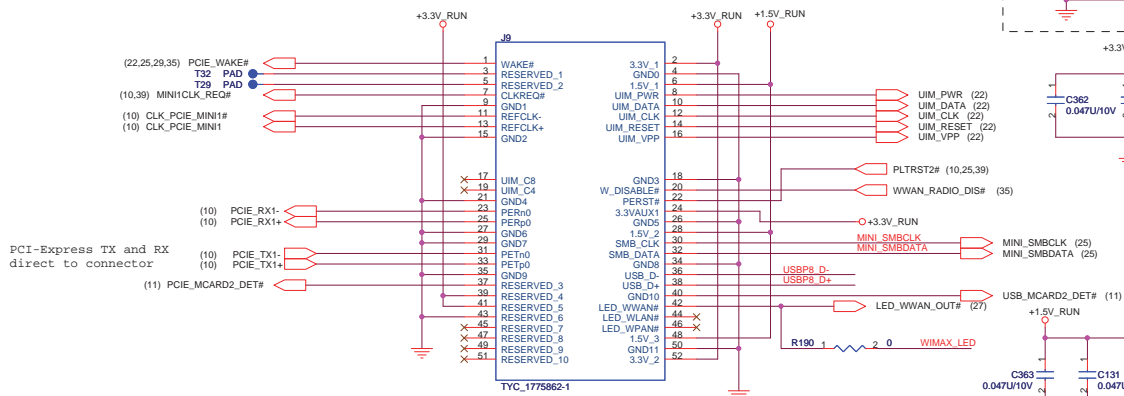
MiniCard WLAN connector



Support for WoW

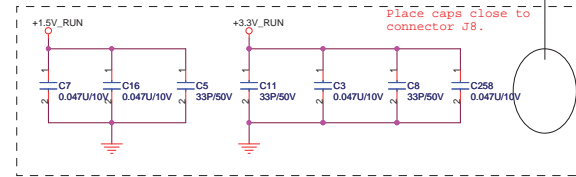
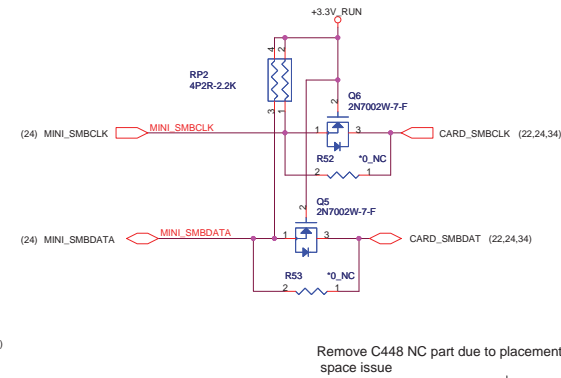
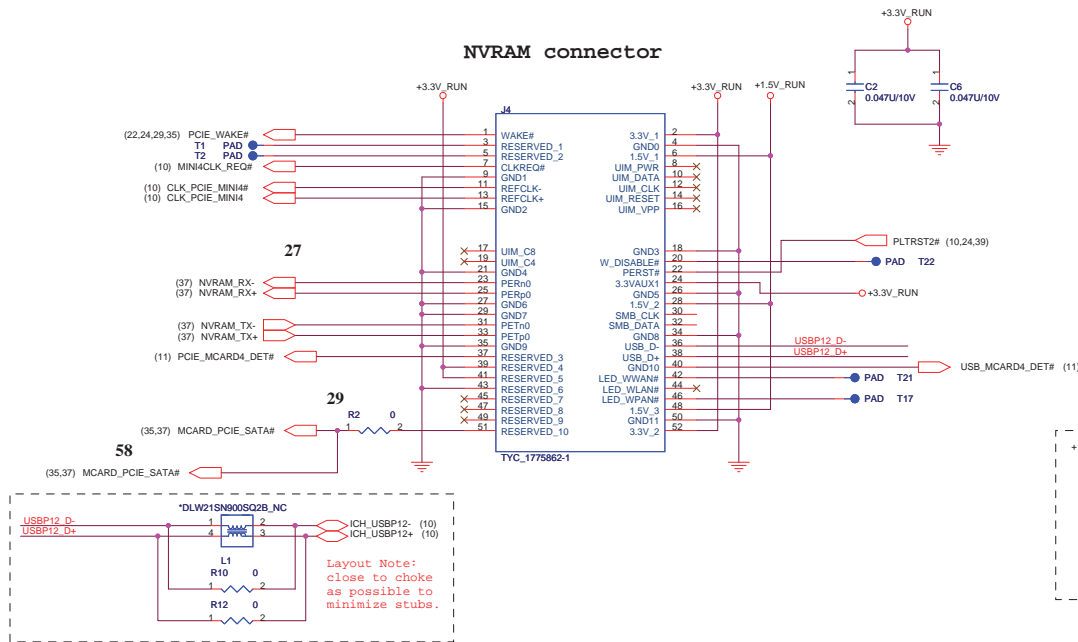


MiniCard WWAN connector

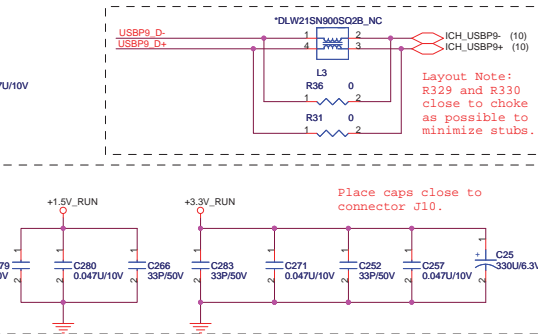
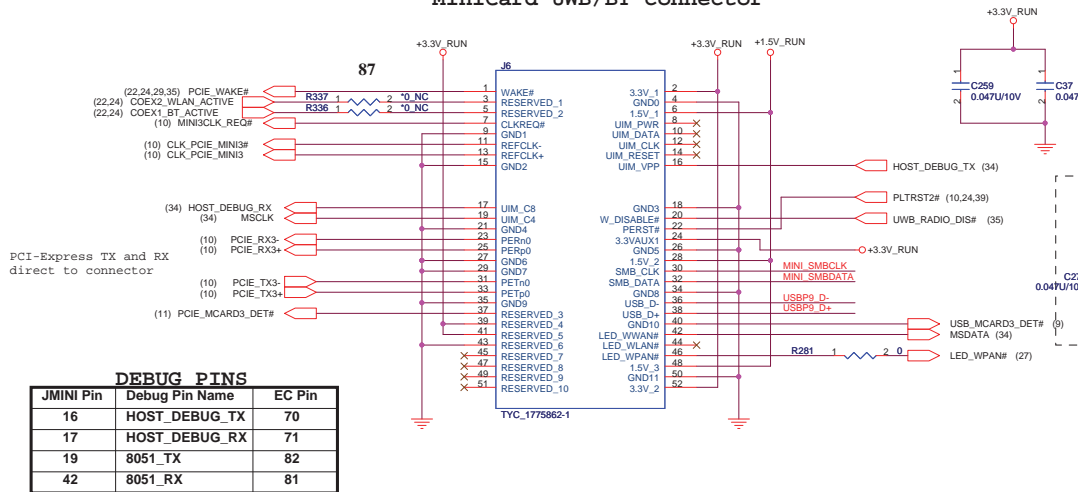


Sim card circuit moves to IOR.

NVRAM connector

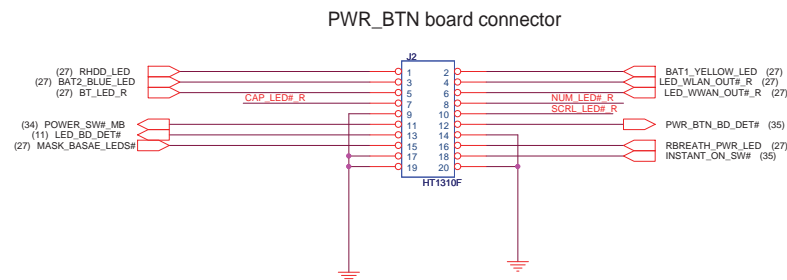
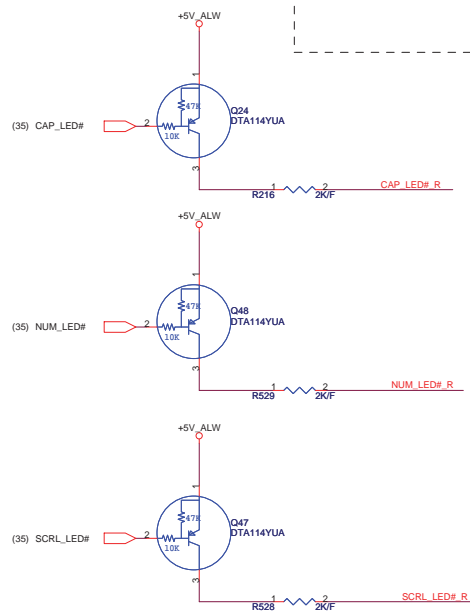
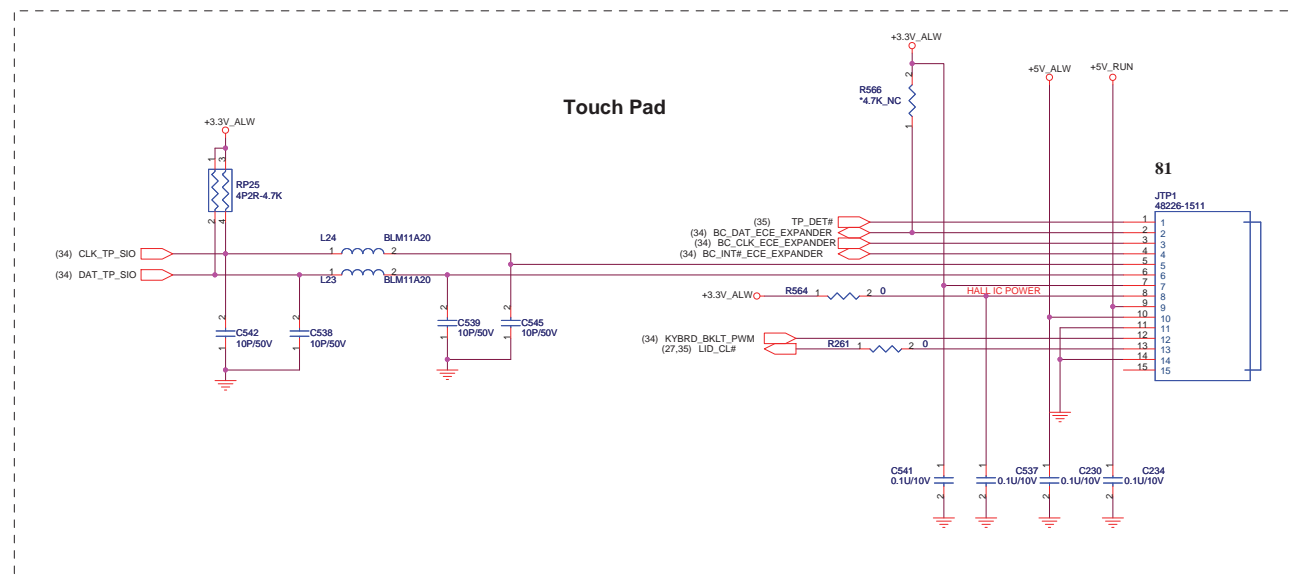


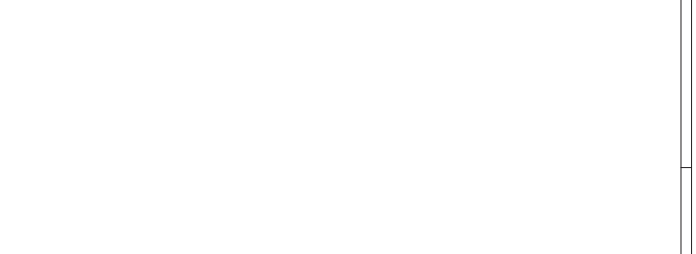
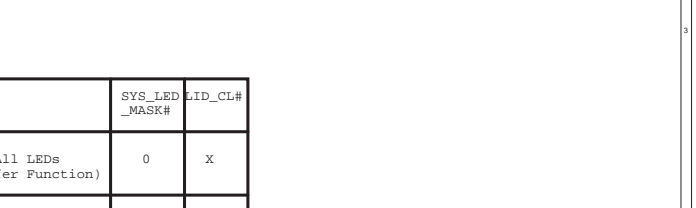
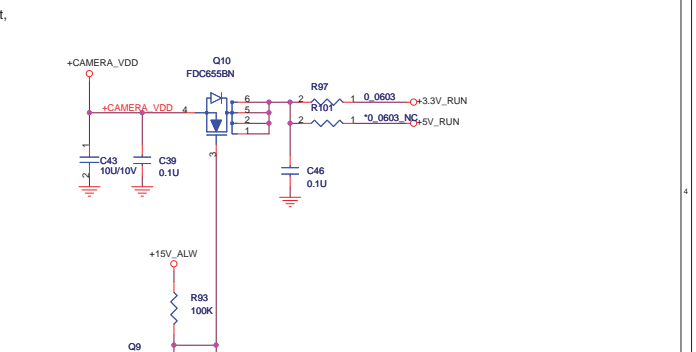
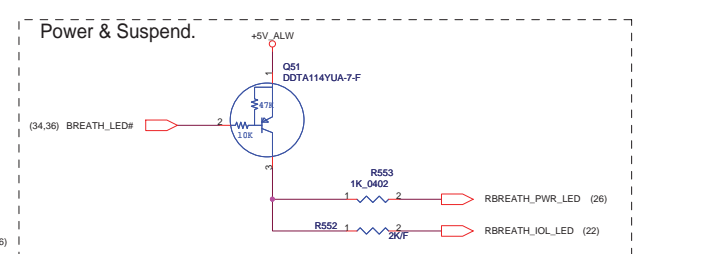
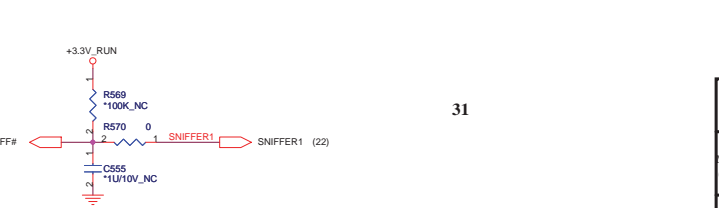
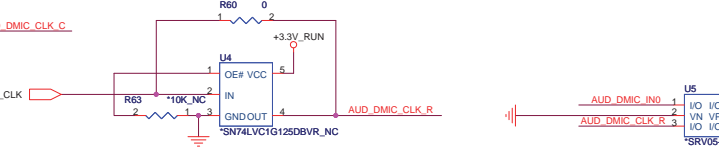
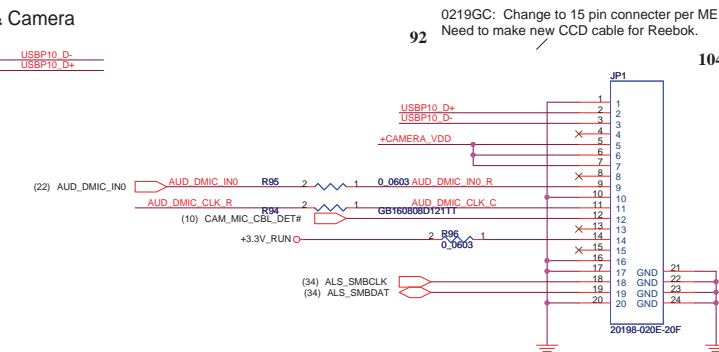
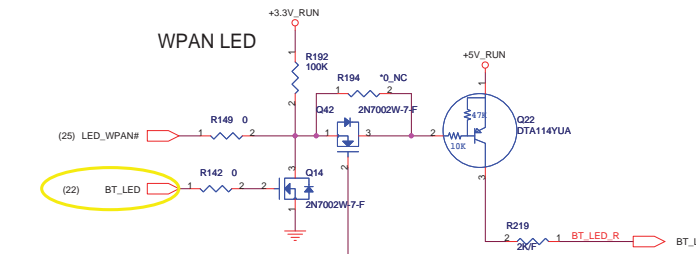
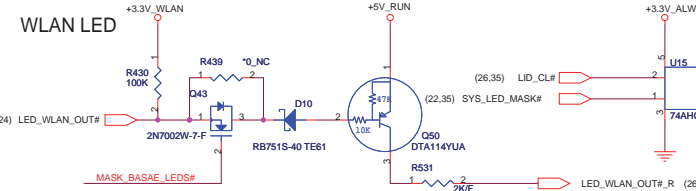
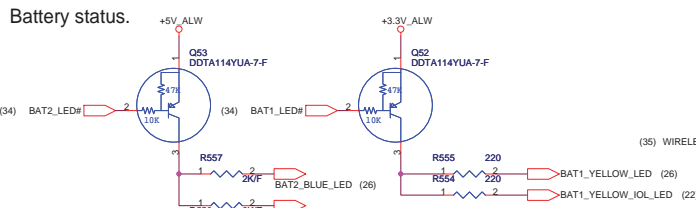
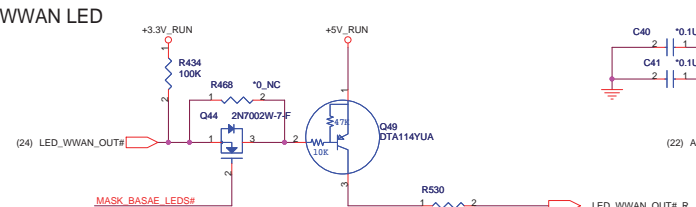
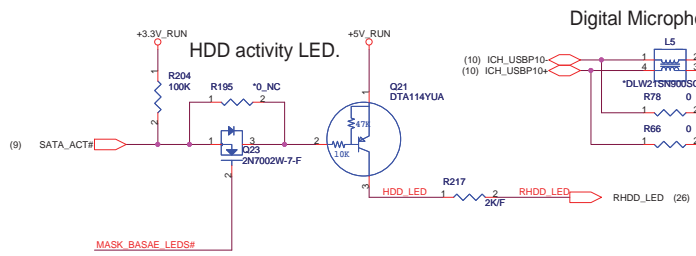
MiniCard UWB/BT connector



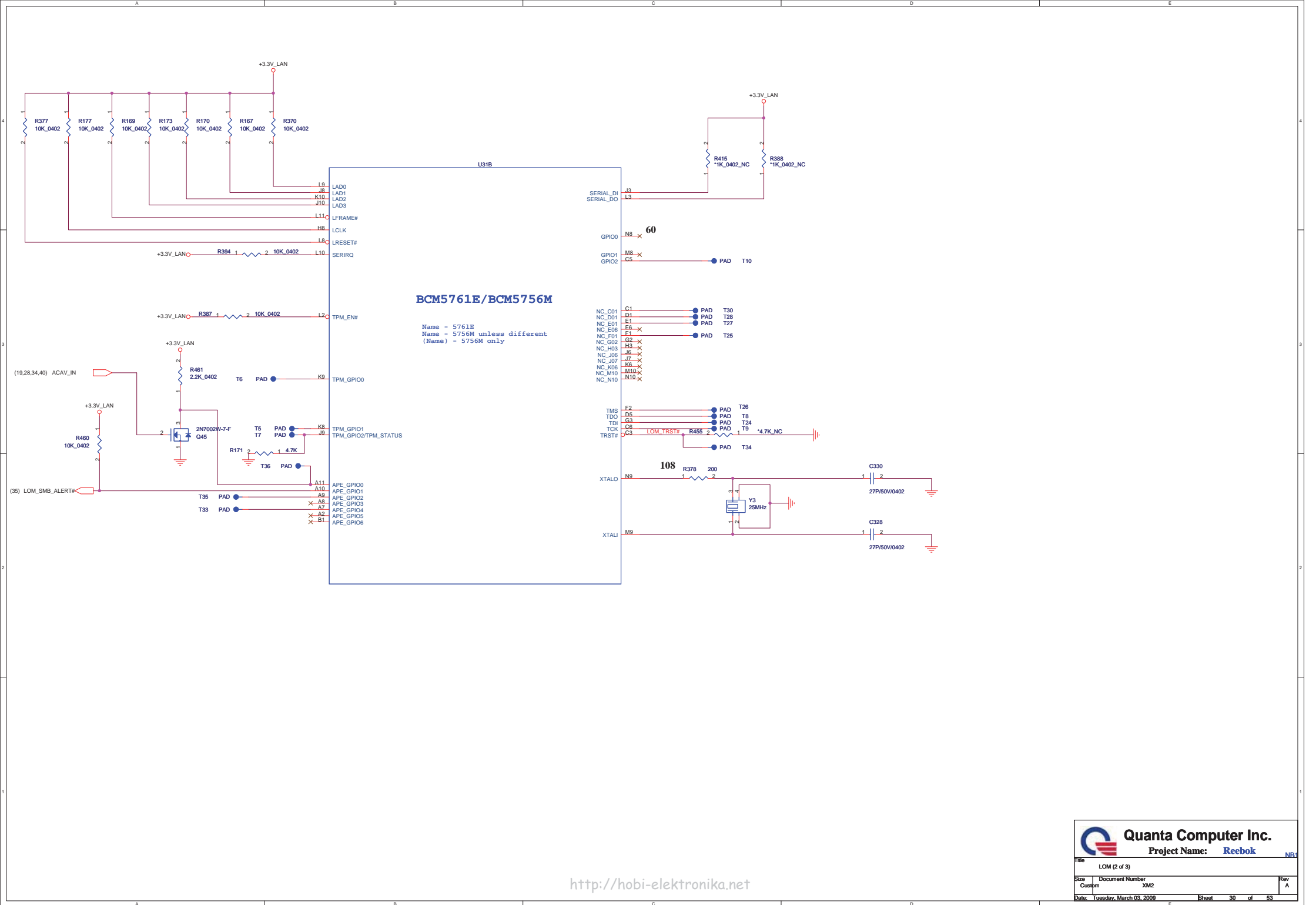
DEBUG PINS

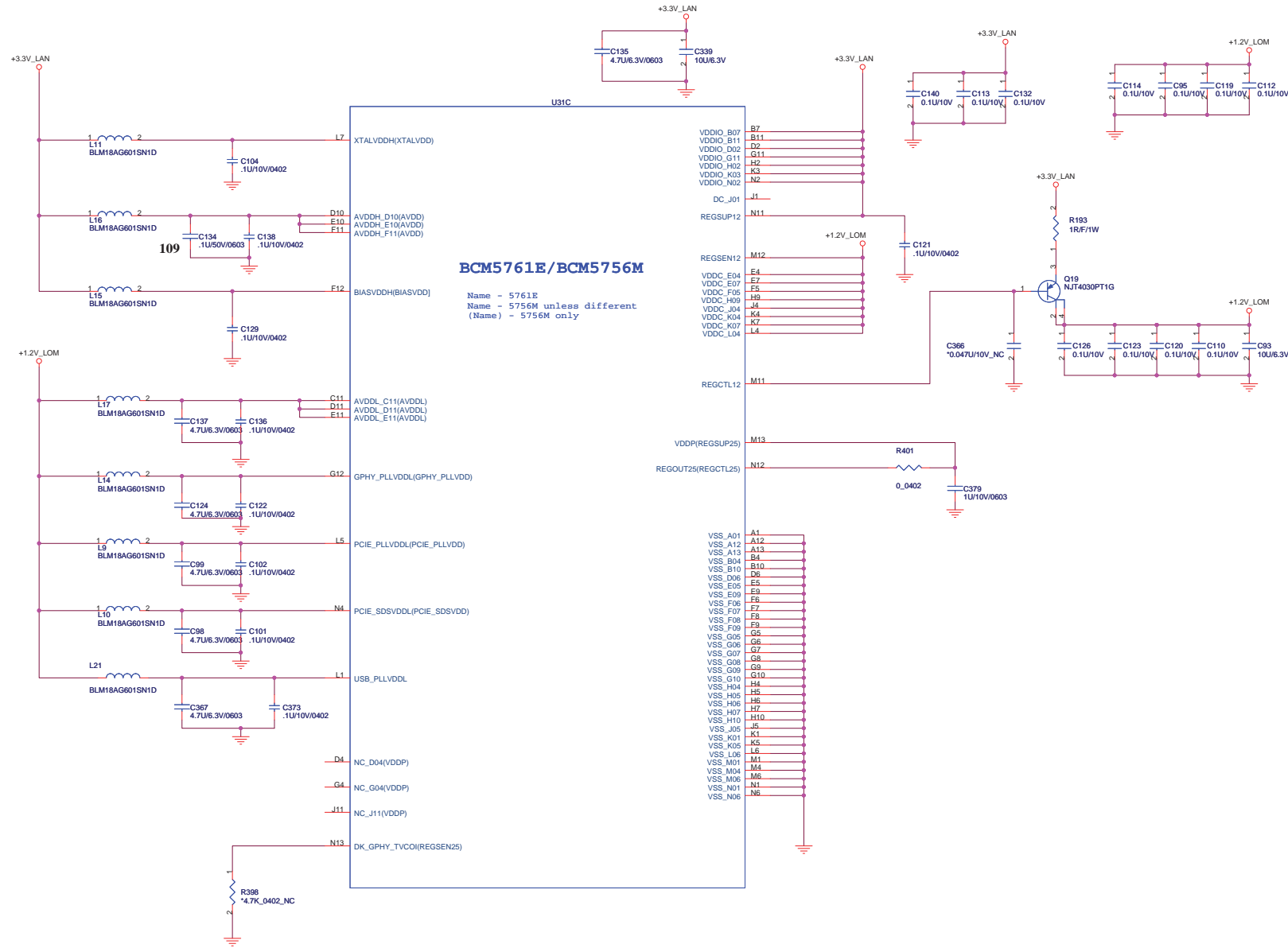
JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

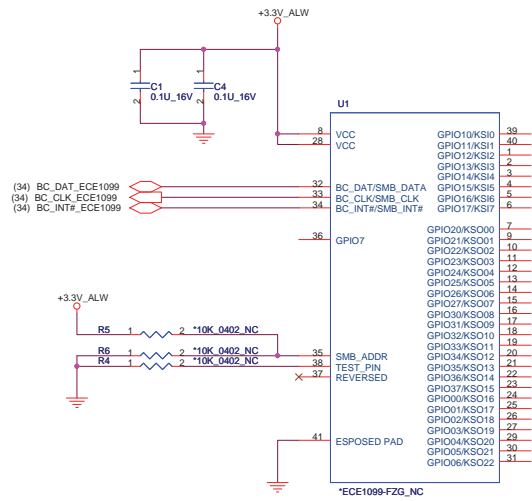


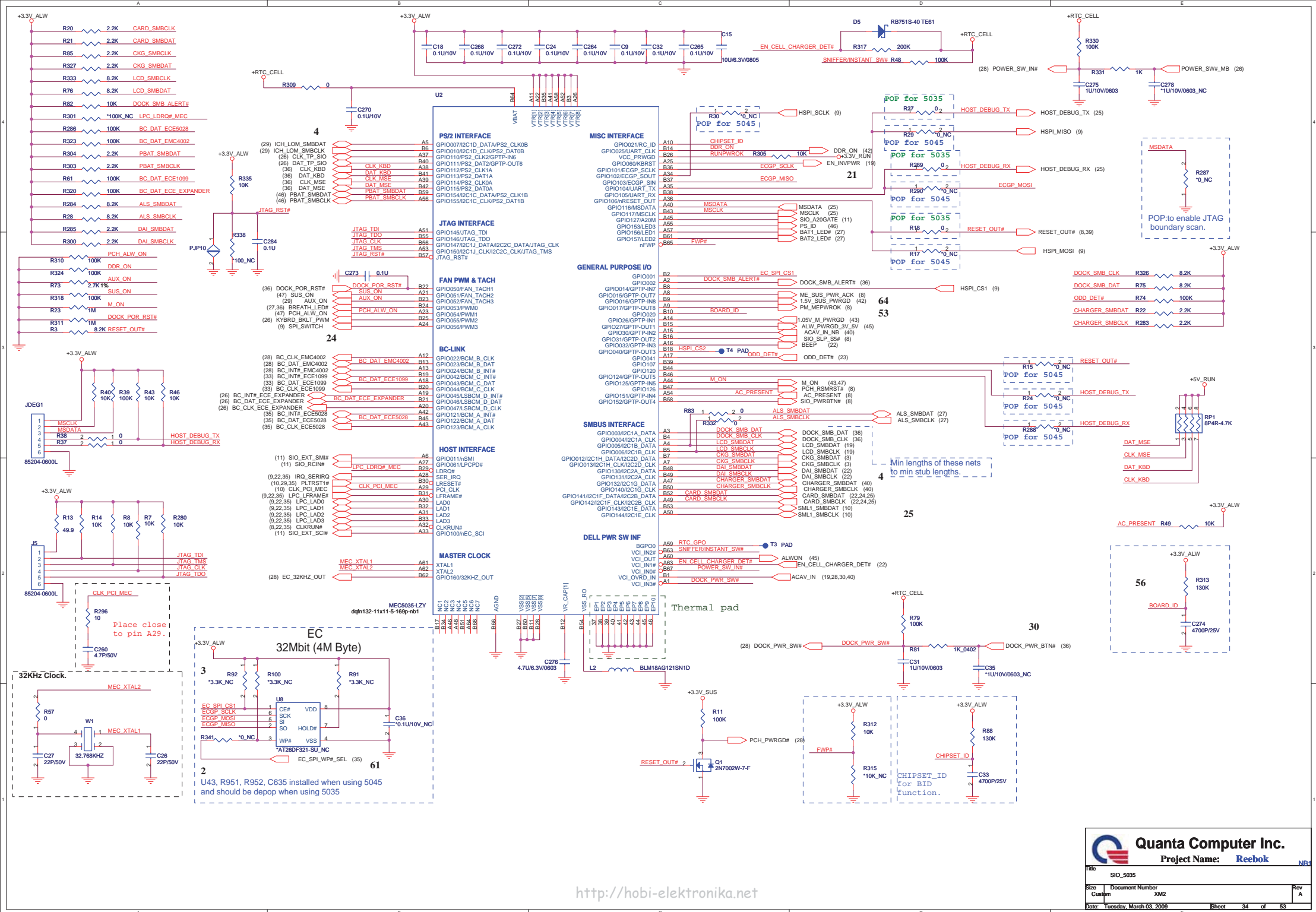


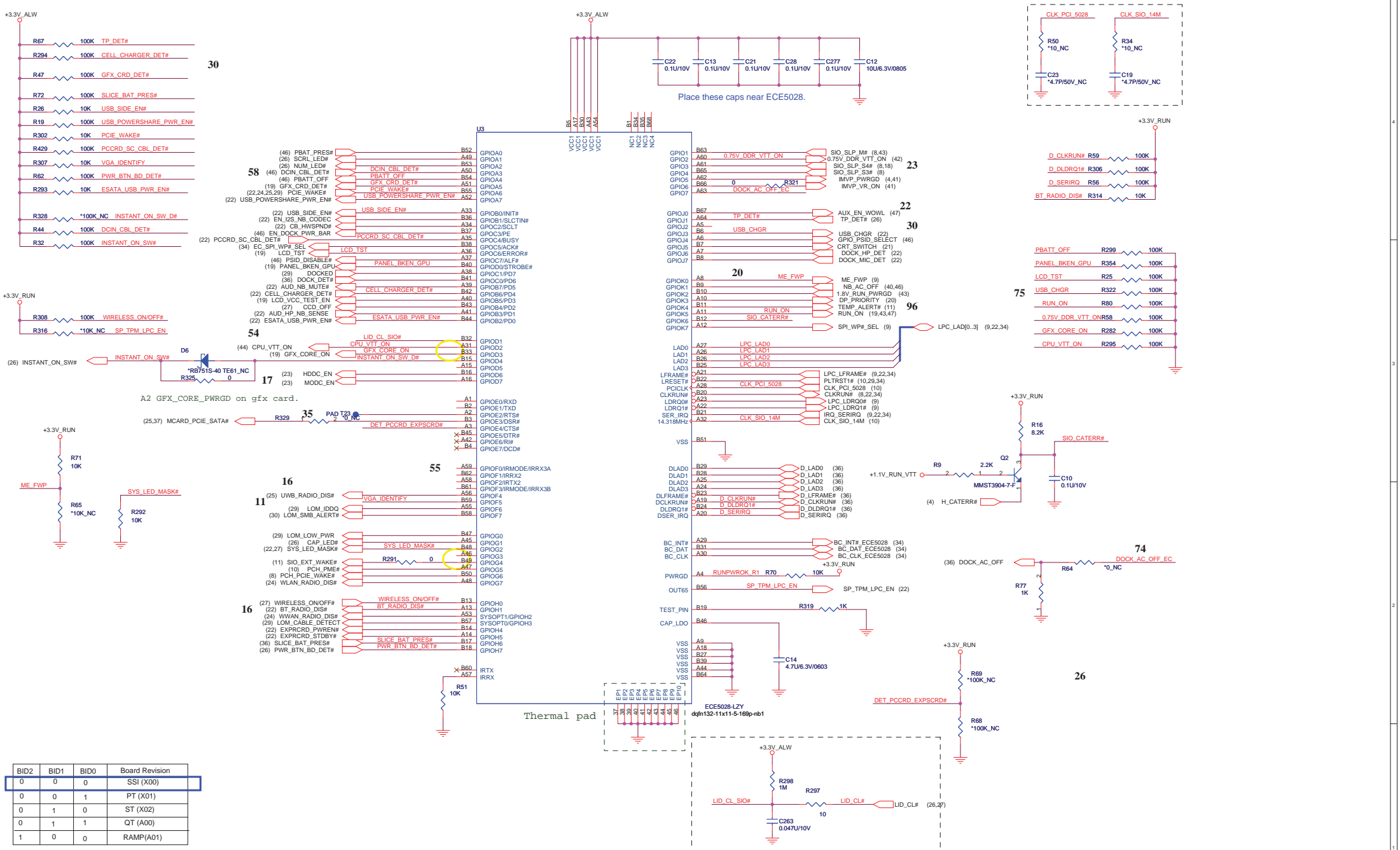
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base LEDs (Lid Closed)	1	0
Do Not Mask LEDs (Lid Open)	1	1



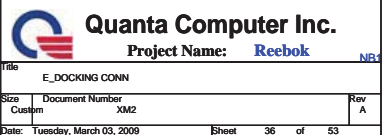




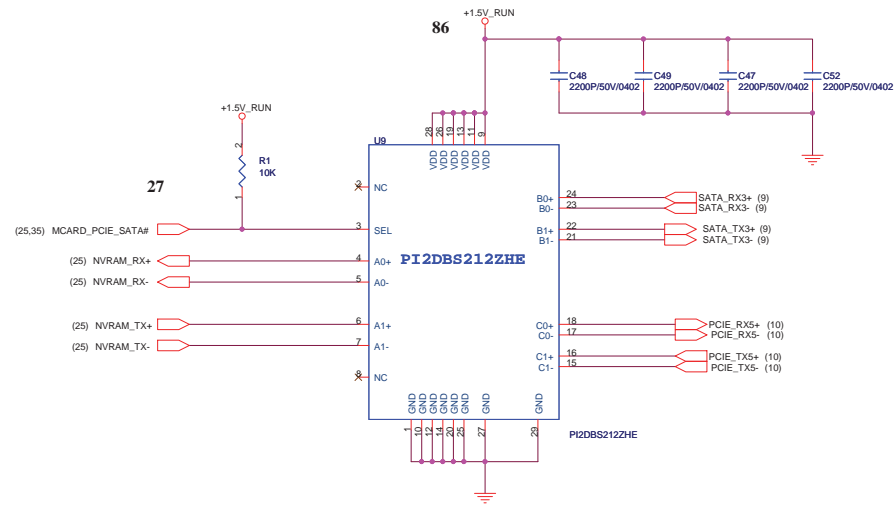




BID2	BID1	BID0	Board Revision
0	0	0	SSI (X00)
0	0	1	PT (X01)
0	1	0	ST (X02)
0	1	1	QT (A00)
1	0	0	RAMP(A01)




NVRAM MUX IC



Function	SEL
Port A to Port B	L
Port A to Port C	H

	1	2	3	4	5	6	7	8
A								
B								
C								
D								

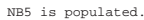


Quanta Computer Inc.

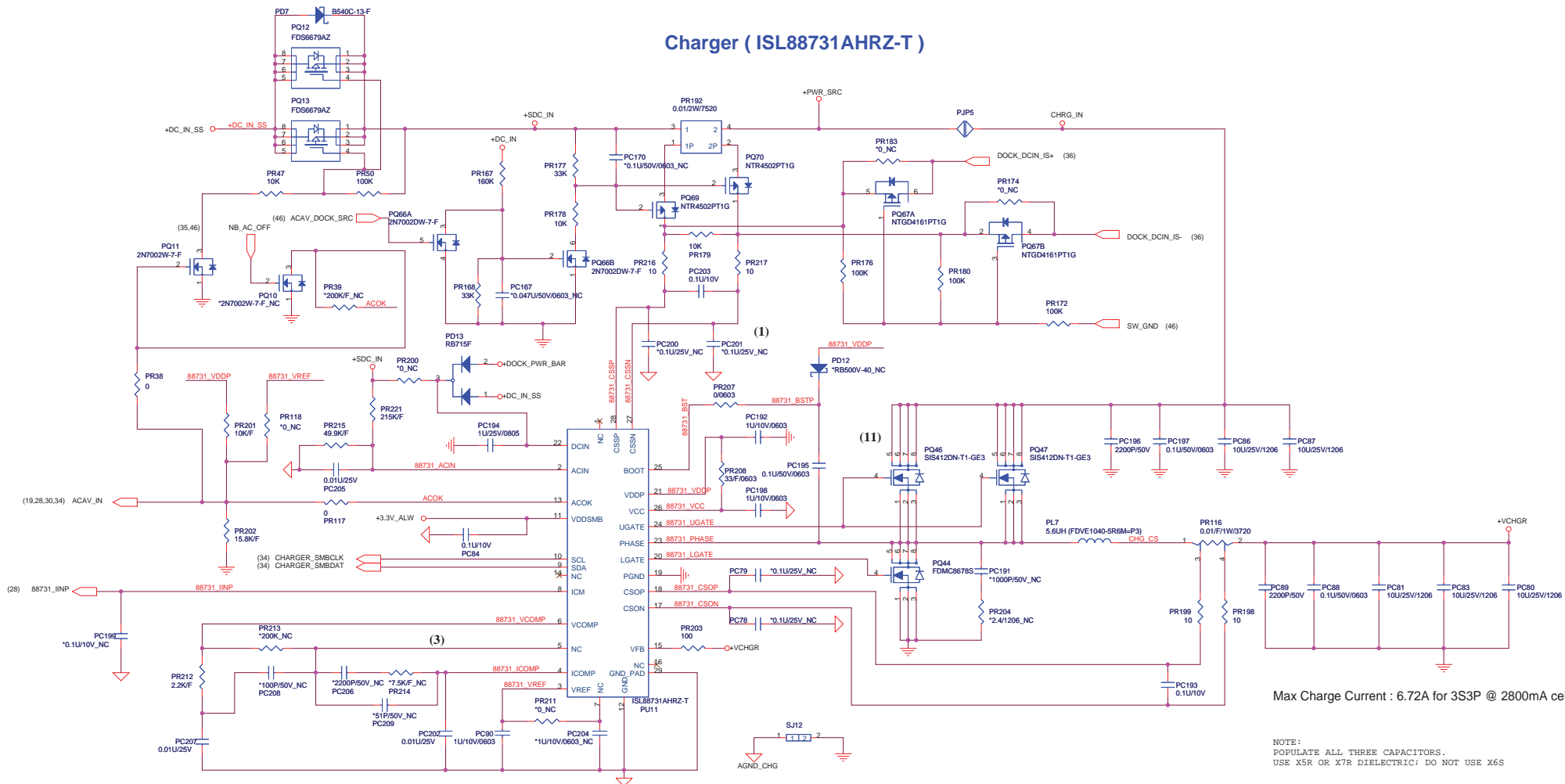
Project Name: **Reebok**

Title	System Power Good		Rev A
Size	Document Number		
	Custom	XM2	
Date:	Tuesday, March 03, 2009	Sheet	38 of 53

CN1

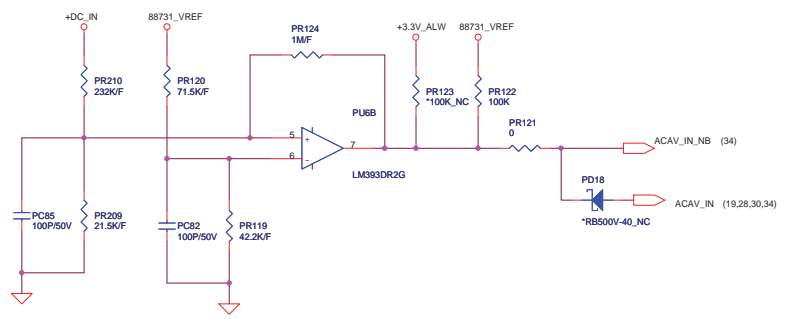
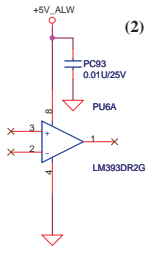


Charger (ISL88731AHRZ-T)

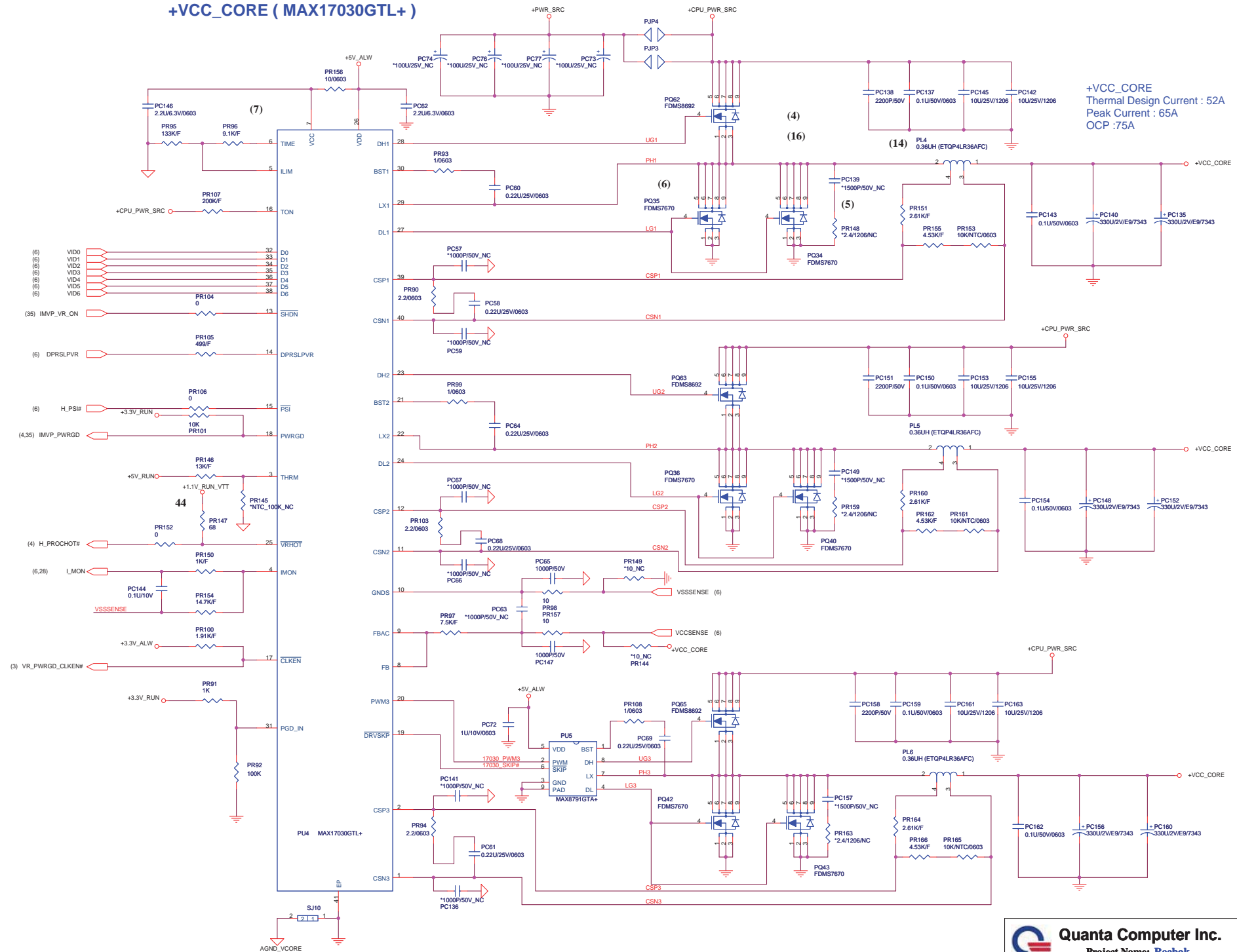


Max Charge Current : 6.72A for 3S3P @ 2800mA cell

NOTE:
POPULATE ALL THREE CAPACITORS.
USE X5R OR X7R DIELECTRIC; DO NOT USE X6S

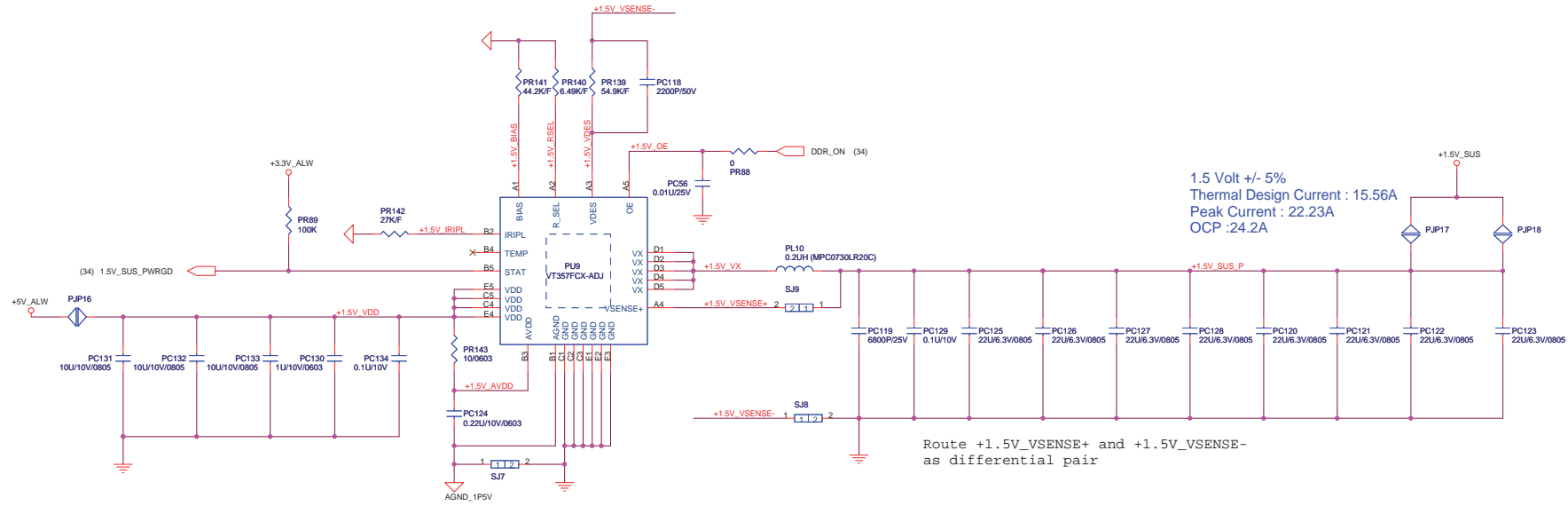


+VCC_CORE (MAX17030GTL+)

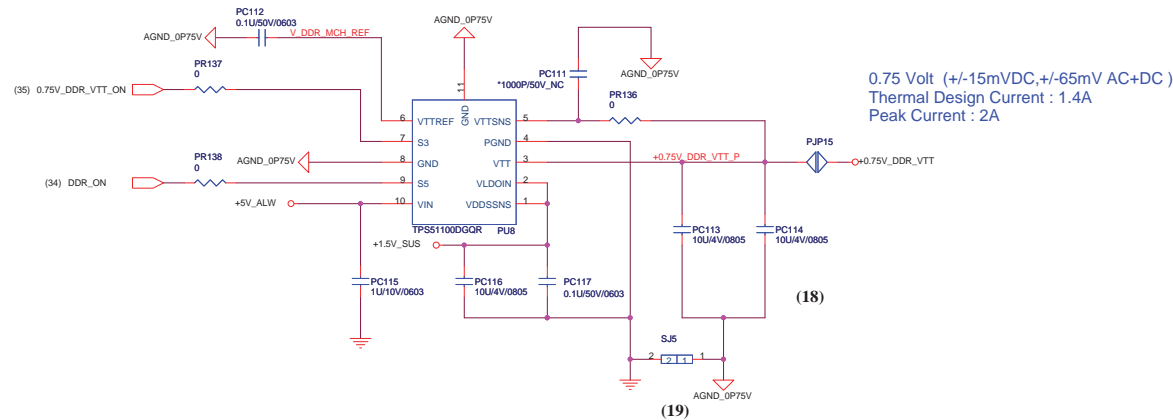


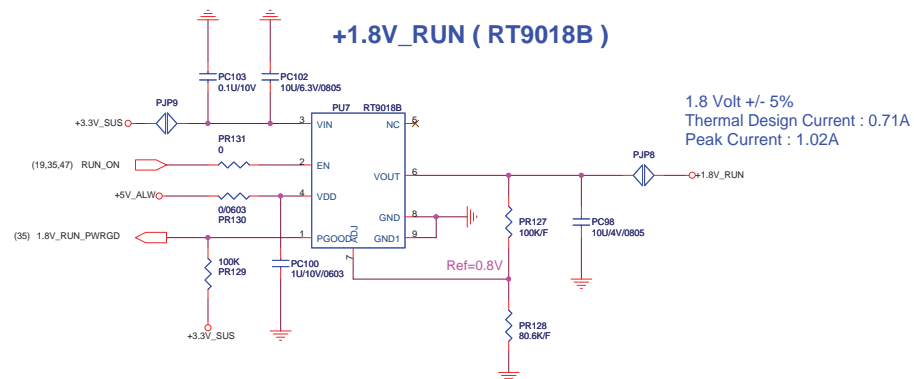
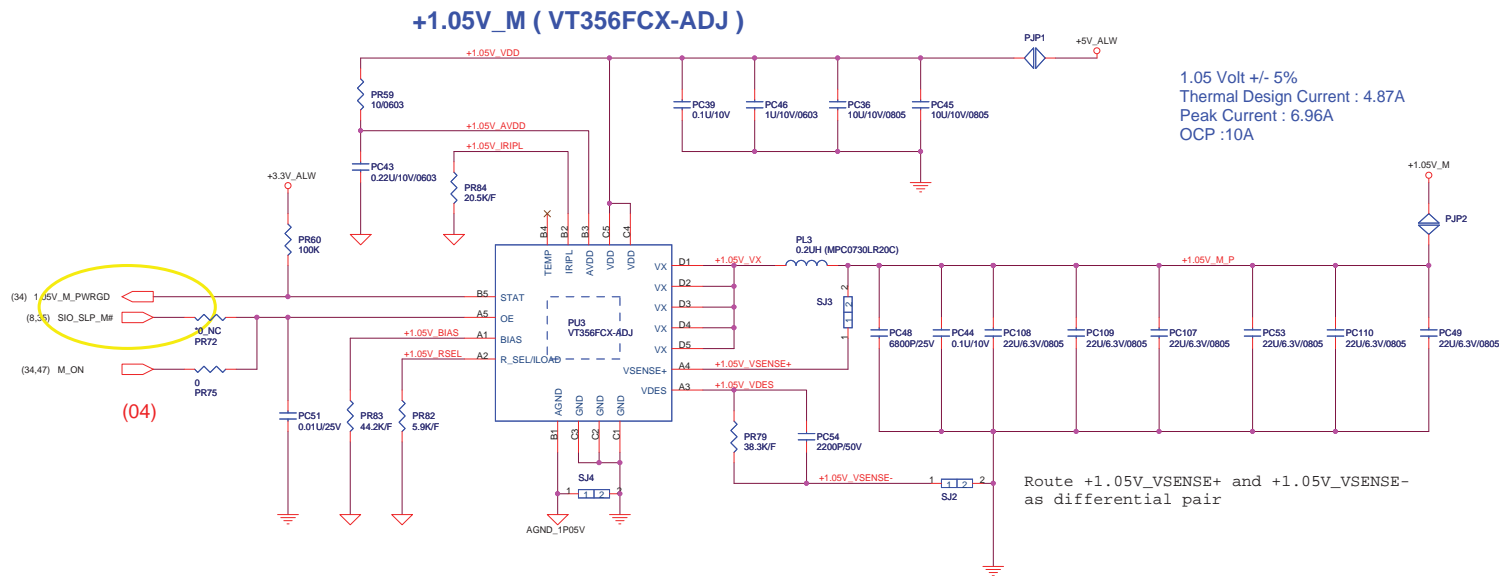
+VCC_CORE
Thermal Design Current : 52A
Peak Current : 65A
OCP :75A

+1.5V_SUS (VT357FCX-ADJ)

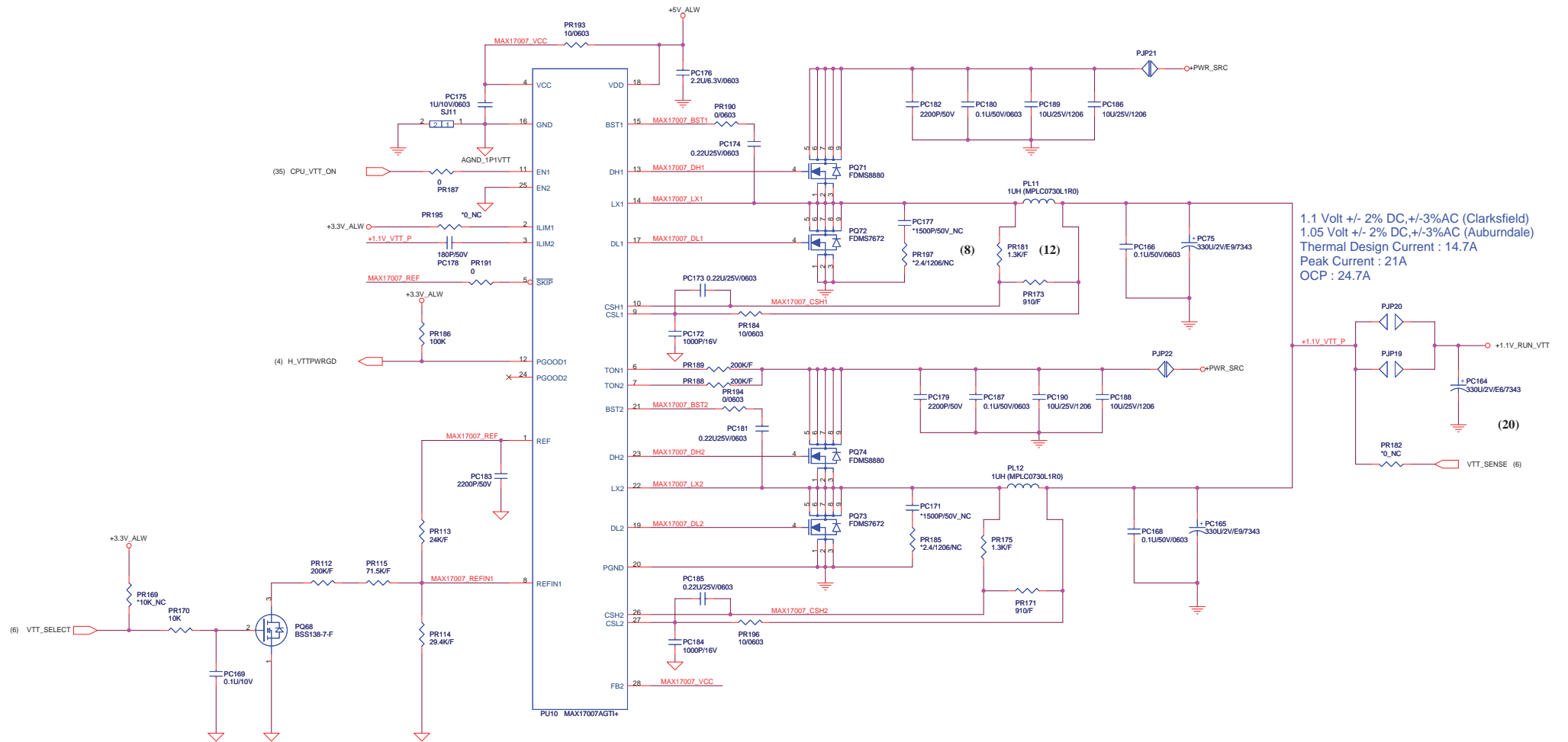


+0.75V_DDR_VTT (TPS51100DGQR)





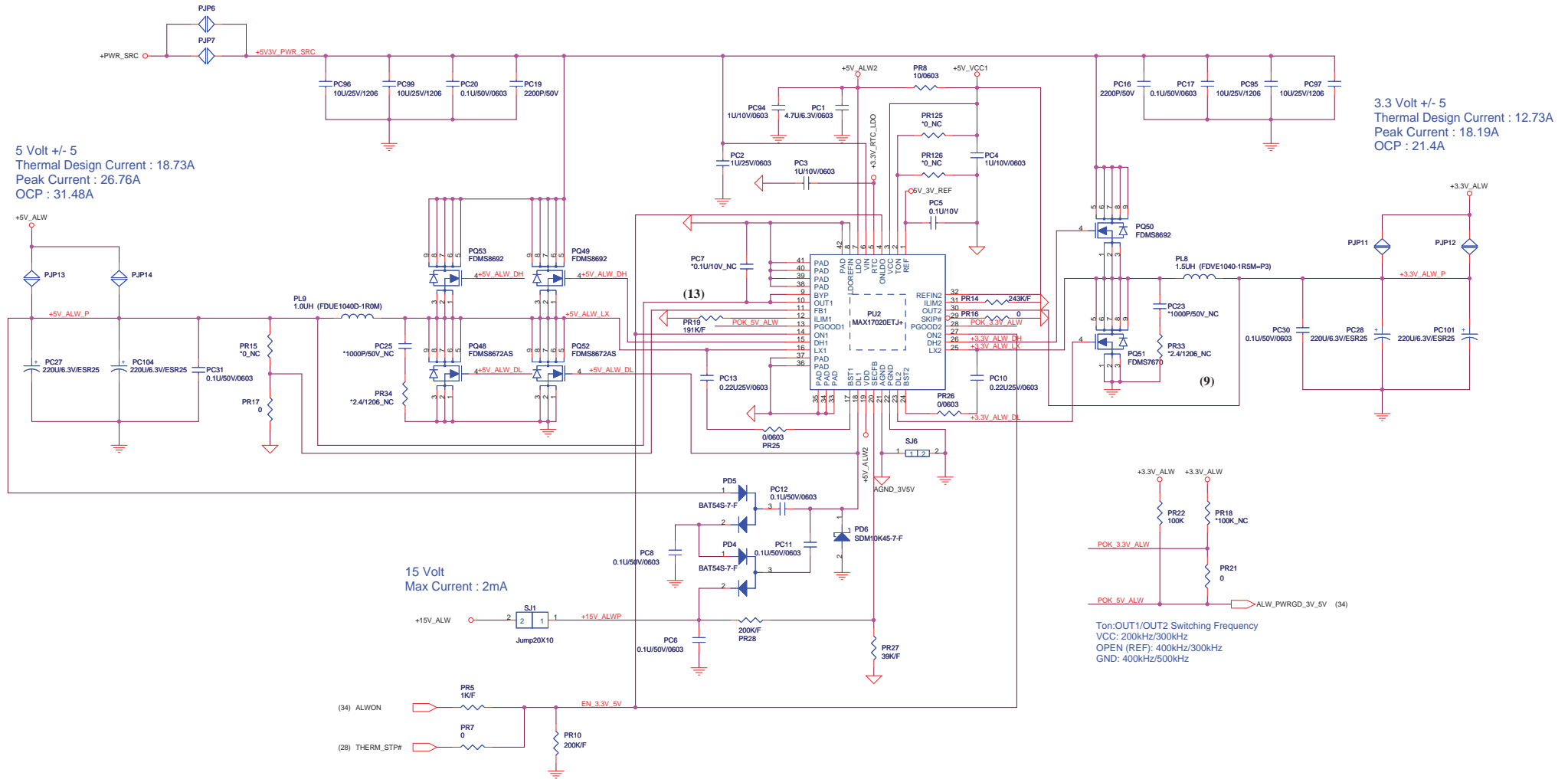
+1.1V_VTT/+1.05V_VTT (MAX17007AGTI+)



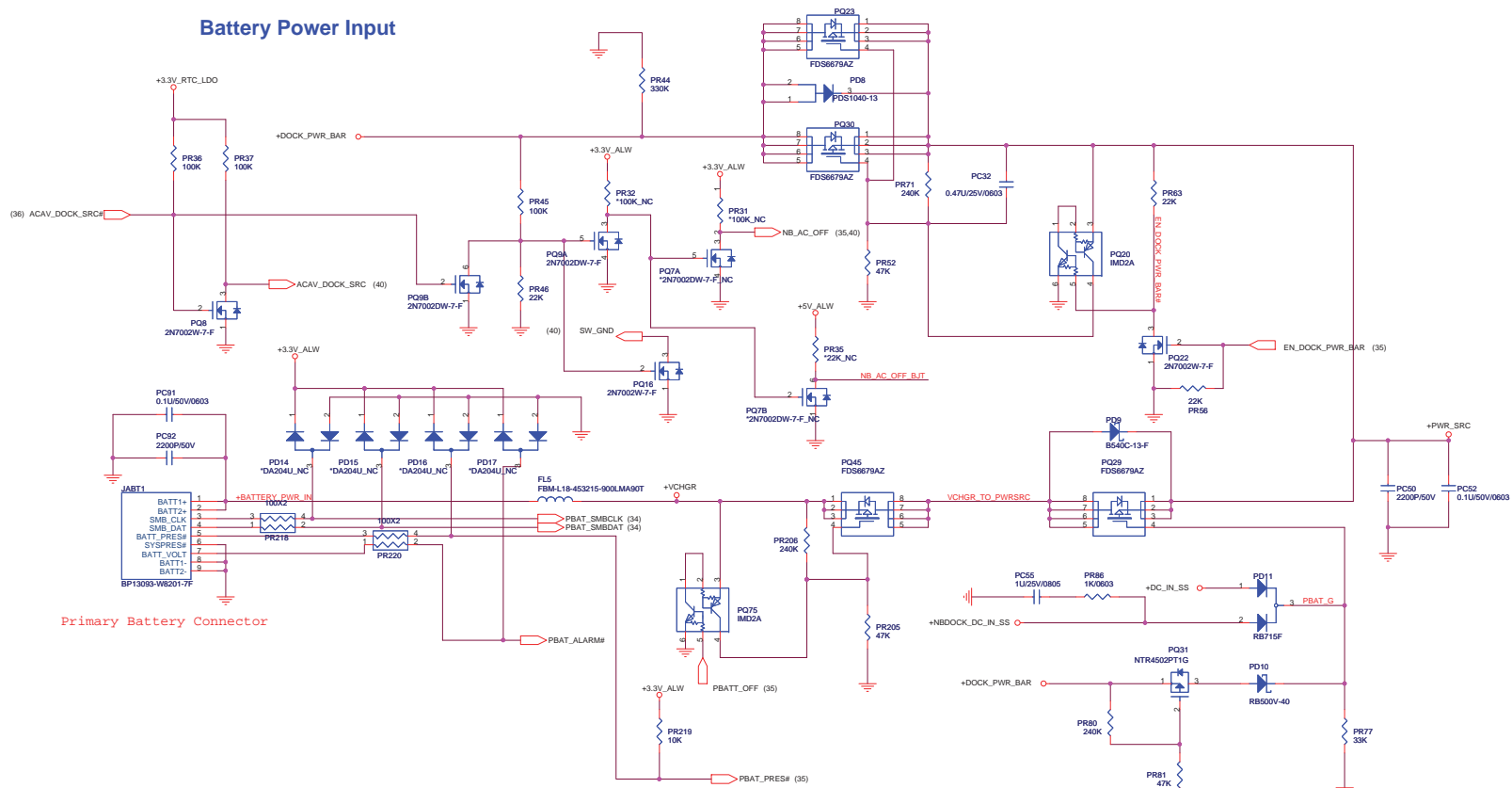
VTT_SELECT = "1", Vo = 1.05V
VTT_SELECT = "0", Vo = 1.1V

1.1 Volt +/- 2% DC, +/-3%AC (Clarksfield)
1.05 Volt +/- 2% DC, +/-3%AC (Auburndale)
Thermal Design Current : 14.7A
Peak Current : 21A
OCP : 24.7A

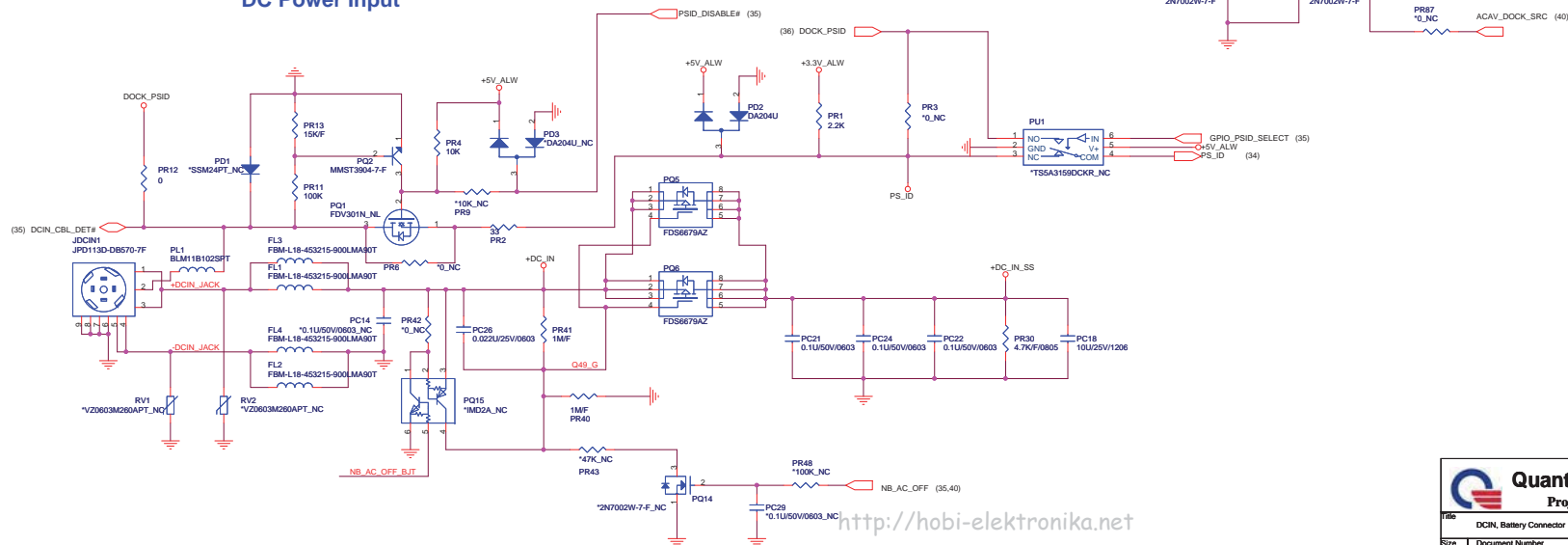
+3.3V_ALW & +5V_ALW & +15V_ALW (MAX17020ETJ+)

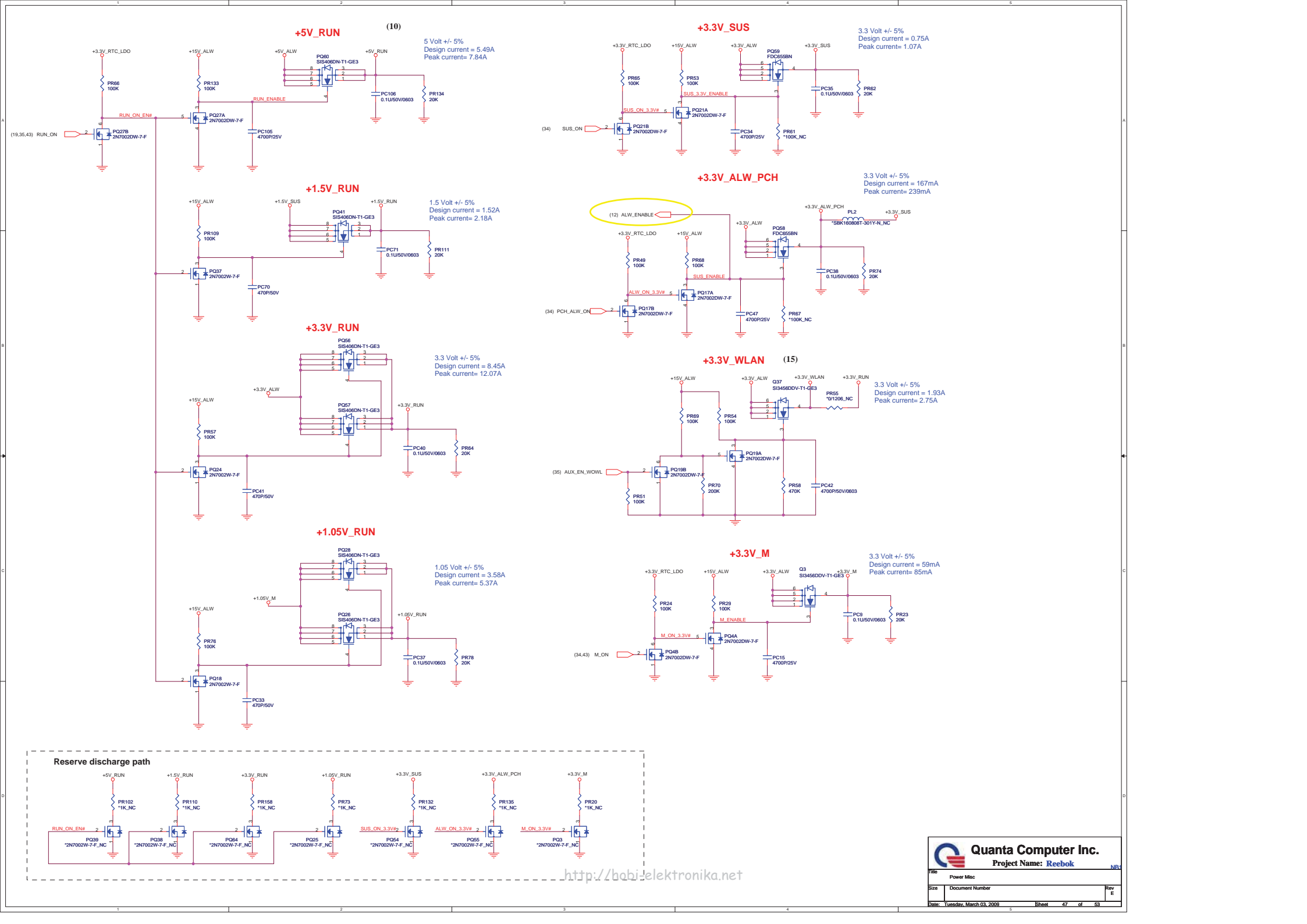


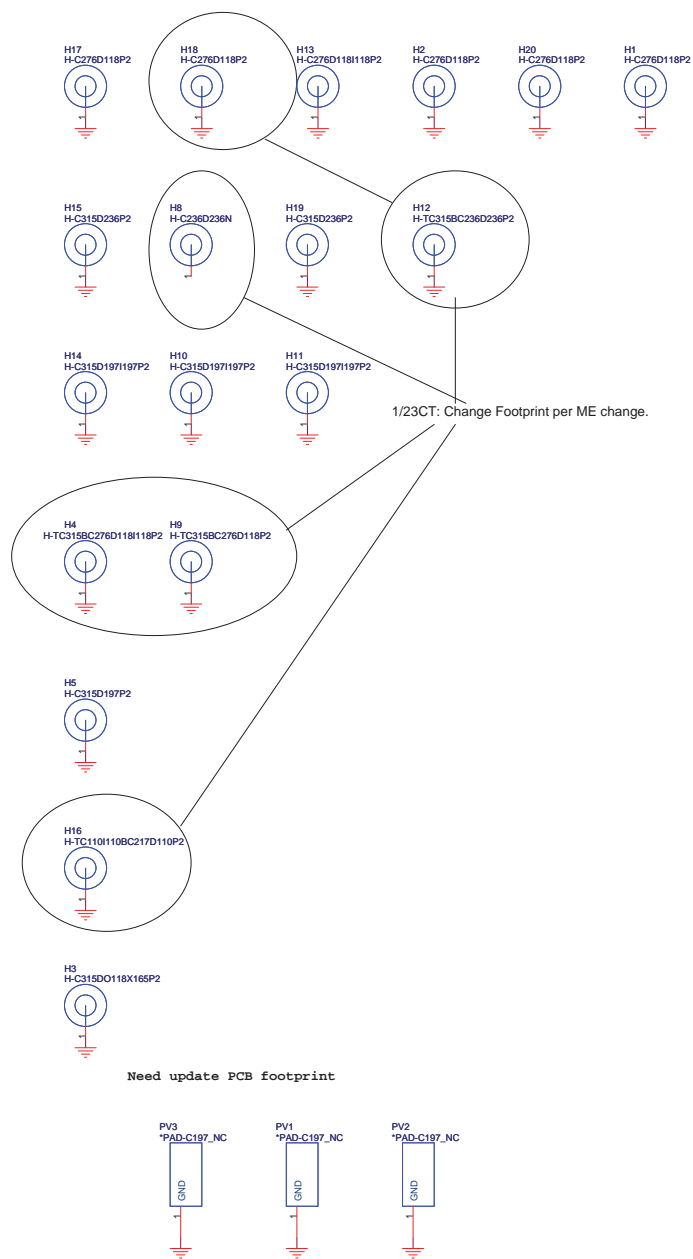
Battery Power Input



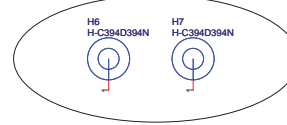
DC Power Input







These 2 holes for Dock holes.



1/23CT: Change Footprint per ME change.

Need update PCB footprint

